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# Design A New Stable And Low Power Bandgap Reference Circuit Based On Fin-FET Device

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**ABSTRACT:** This paper describes the design of a bandgap reference, implemented in 32 nm FinFET technology. The paper introduced new method for increasing stability of output voltage of bandgap circuit. In the proposed architecture extra feedback is used for setting the output voltage in fixed voltage. This feedback makesbandgap circuit more stable and speedy employing back gate biasing of the FinFET devices. This circuit generates a reference voltage of 300mV and has a variation about 0.041% versus temperature in TT corner. High gain OTA utilized in the feedback loop was designed by innovative bulk FinFET devices. FinFET OTA used in this work is very low power and high speed compared to conventional CMOS designs.It was tested with supply voltages between 0.7 and 0.9volt and between -40°C and +120°C. The variation of output voltage versus VDD variation is lower than 0.01% in TT corner. This circuit works in a current feedback mode, and it generates its own reference current, resulting in a stable operation. For resistor and diode connected transistor the technology elements were used instead of ideal components. The technology in use is 32 nm PTM.

**Keywords:** Bandgap reference, current feedback, FinFET, startup circuit, VDD variation

## 1 INTRODUCTION

A very popular element in each integrated circuit(IC) which is required for some application such as power management, data converters, voltage regulators and memories is a Bandgap Reference (BGR) circuit. There are a lot of research in designing low power digital and mixed signal electronic systems[1-3]. Its high stability against temperature and voltage variation is very favorable in every digital design. It could be designed by a couple of Bipolar Junction Transistors (BJT) which operate at different current density have different base-emitter voltage-each of them related to temperature. Voltage deference between the emitter of these pair of BJTs is not related to temperature or in the other words has zero temperature coefficients. For example for establishing a high precision ADC a critical part is the bandgap reference voltage. The basic of bandgap is related to two BJTs with different current density. Their difference makes it easier to cancel the negative temperature dependence of a simple PN junction and replace it with positive temperature dependence of a PTAT circuit which embodies some other elements a constant DC voltage is generated. This circuit can be designed such as the temperature dependence of the whole circuit was in propinquity to zero. Some innovative techniques are used to decrease this voltage so as can be scaled down with the technology scaling. One of them is the use of resistive subdivision technique with native transistors or diodes[4-6]. Some new techniques use a new technology for implement analog circuit such as FinFET based bandgap[7]. Some of other technique partially forward biases the PN junction of source bulk of PMOS transistors. Another example of 1V bandgap circuit uses the sub threshold region of transistors as a low voltage source or uses the differences between work functions material of gates for transistor with different doping concentration and types [8]. In order to implement lower than 1V bandgap circuit some others use the dynamic threshold MOSFET [8, 9]. However scaling down the reference voltage of the BGR results in lower noise resistance of the circuit some chopper stabilizing technique can be used to lower the noise of supply voltage and it should be considered as a tradeoff between supply voltage and noise resistance [10-12]. There more problems in order to design BGR in FinFET technology rather than conventional CMOS structures. It is due to difficulties of fabricating the diodes in thin SOI layer. Another disadvantage of the FinFET is that it is very hard to implement resistors which have low area in the process employing only metal gate.A single ended Op-AMP is required to fix the drain voltage of MOS transistor. The structure of Op-Amp is fully discussed in this paper. Other details about each parts of the work consist of hand calculations about the circuit, transistor level and waves are also totally concerned and archived in this paper.

## 2 FINFET

Wells are omitted in FinFETs with SOI technology. There is no source-well diode as a parasitic BJT in the implementation of the BGR and so-called lubister diodes are used as replacement to them [13]by sticking the poly to the ground junction [14]. A lubister'spn junction is shield from silicidation by oxide by gate material layer. In other word the pn-juction is protected from being short circuit. Background doping can certainly maintain the just below the shield material as non-intrinsic[7]. This paper introduces an innovative topology in order to increase the accuracy and stability of the BGR. The low power characteristics of FinFET entitle the use of SOI devices besides its sharper subthreshold slop and quicker BGR design. The FinFET based BGR has tendency to respond quicker to external changes in voltage and current rather than the conventional CMOS BGR.FinFET devices have the tendency to shrink without the subsequent scaling effects. So they are a good substitute for the conventional bulk devices. As shown in Figure 1 the FinFET has two gates which can be biased separately or shared. The first is called independent gate and the second is called common gate. The first type can be used for Dynamic Body Biasing (DBB) for controlling the threshold voltage of the channel during the operation or at the design time. The latter type can also have more control over the channel with sharper subthreshold slop. FinFET devices also have multiple advantages with respect to conventional bulk MOSFETs in suppressing Short Channel Effect (SCE). Self-aligned structure and source/drain underlap allow single lithography and etch step in fabrication of FinFET [15] and better performance respectively[16]. The new 32nm technology is used and its characteristics are archived in Table 1. This paper is about designing a FinFET bandgap in transistor level. The FinFET is a widely used technology because of its low power high gain and low/moderate frequency of operation with suppressing the short channel effect (SCE). Self –aligned gates in FinFET results in single

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lithography and etch step in fabrication of the IC. Indeed underlap source/drain FinFETs show enhanced performance. The usage of this device is very attractive in now-a-days portable devices like cellular phones, wireless receivers and biomedical instruments. Several characteristics in design by FinFET should be conside3red to have process independent and high performance design [17-19].

**Table 1.** FinFET Parameter in 32nm technology

| | |
|---|---|
| $L_G$(nm) | 32 |
| $T_{ox}$(A) | 14 |
| $T_{si}$(nm) | 8.6 |
| $V_{DD}$(V) | 0.9 |
| Channel Doping, $N_{BODY}$ (#/cm$^{-3}$) | $2\times10^{16}$ |
| $H_{fin}$ (nm) | 40 |
| $V_{t0,nmos}$(V) | 0.29 |
| $V_{t0,pmos}$(V) | -0.25 |

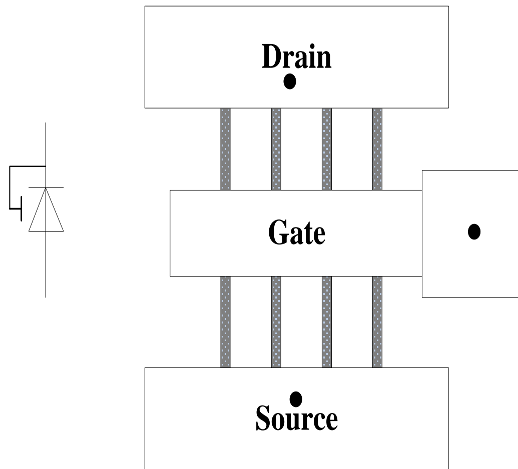


**Figure 1.** Lobster structure

## 3 PROPOSED ARCHITECTURE OF THE BANDGAP

This paper introduces an innovative topology in order to increase the accuracy and stability of the BGR. This topology can regulate the output voltage variation by changing the core current of the BGR and stabilize the output node's voltage. The back gate of the PFET in the main body (M3) is biased by a feedback circuit which senses the output voltage variability due to PVT or even noise variation. The M5 sense the changes in the output voltage and amplify it as a common gate amplifier. This voltage is transferred by an active load as M4 to the back gate of the main PFET (M3) presented in the core branch. In other words, the more increase in the output voltage results in higher voltage in the drain of the sense transistor (M5). The more voltage biases the back gate of M3 increases the absolute value of the threshold voltage; hence the current of the output stage decreases and the output voltage fall down until it reaches the desired value. The ratio of the M4 to M5 should be chosen in such a way that they produce proper voltage of biasing the back gate of M3. The higher gain employed in this pair of transistor can sense even negligible change in the output voltage and regulate it in order to change the current of the M3. This can strongly increase the accuracy of the output voltage accosting with PVT and noise changes. A BGR is created by addition of two voltages that one of them is negatively related to temperature while other has positive temperature coefficient. Proper multiplication weight is found by tuning the resulted voltage in different temperature. The difference between multiple VD of two diodes changes Proportional to Absolute Temperature (PTAT). The PTAT relationship is given by [20]

$$\Delta V_d = V_T \ln\left(\frac{J_2}{J_1}\right) \quad (1)$$

And

$$V_T = \frac{KT}{q}$$

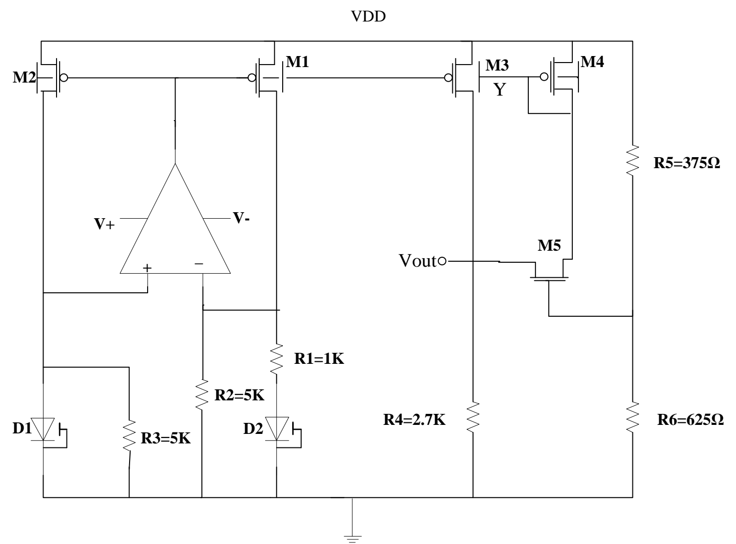


**Figure 2.** Sample circuit of a bandgap which used current mirror approach to decrease supply voltage coefficient

A new method of implementing a BGR is repressing as follow. Whole circuit consist of an independent supply voltage, 2 diode consist of FinFETswhich generate a voltage which decreases as temperature increase some resistor are used to improve the performance.Using a current mirror in top of the BJT will decrease the supply noise in output voltage. It also needs an op-amp whichcompleted the feedback loop. You could see a sample of bandgap circuit inFigure 2. The use of this FinFET could be possible because our sample circuit has diodes. If op-amp is ideal the voltage input op-amp nodes are equal and the voltage deference between diodes will drive the resistor-which are the real resistor technology. So if it is assumed that this resistor is ideal and follows the ohm's law, it could be derived that:

$$R1 = \frac{\Delta V_D}{I_{ss}} \quad (2)$$

And

$$V_{ref} = V_D.\frac{R4}{R_2} + \Delta V_D.\frac{R4}{R1} \quad (3)$$

And the output reference voltage could be set by weighting the $V_{be}$ voltages with resistors' value.

## 4CASCODE OP-AMP

The BGR needs a high input resistance OTA which is implemented in folded cascade to have low input common

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mode voltage.An op-amp is needed to implement the bandgap circuit and complete the feedback loop. In this paper a 1stage high swing folded cascode with DC gain about 1.29K in Typical-Typical corner and 27˚C was designed and was used in the bandgap circuit. Folded cascode is used because of its wide common mode input voltage and low voltage of collector-emitter. The topology of the cascode OTA is depicted in

Figure 3.

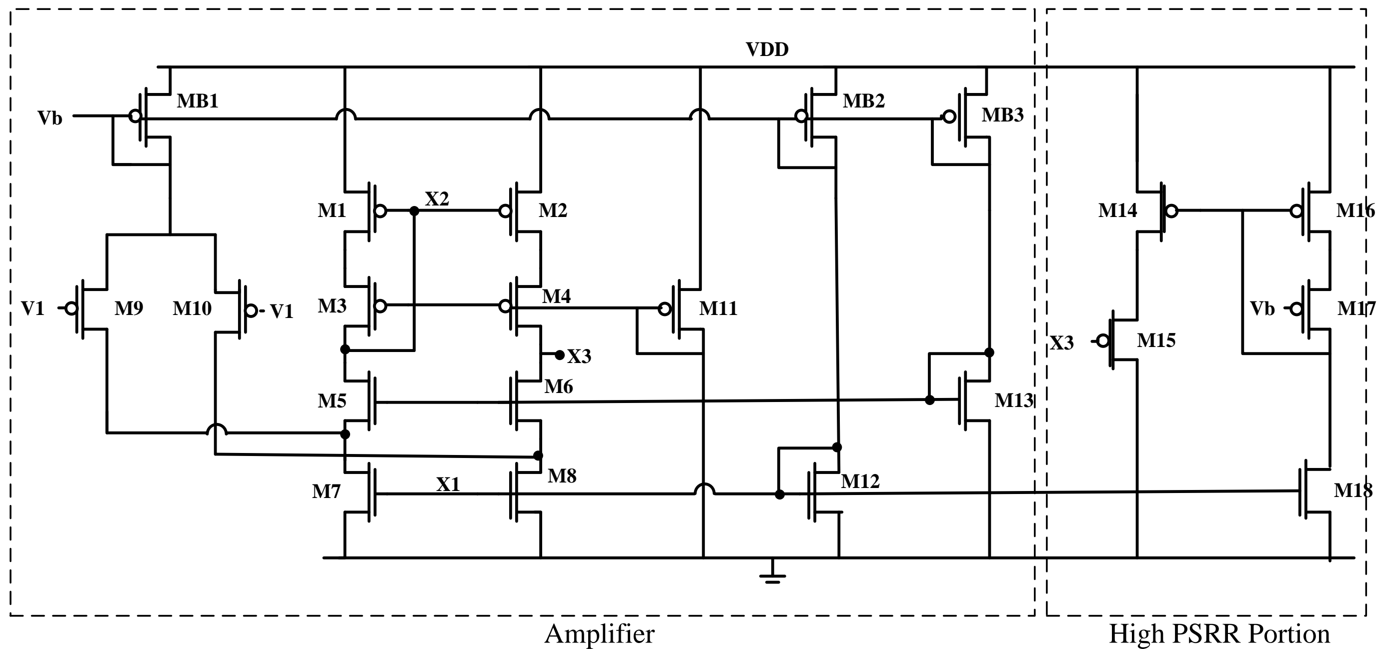


**Figure 3.** Topology of Folded Cascode OTA

OTA has maximum gain in SS corner and -40 °C and minimum gain about 400 in SF corner and 120 °C and in typical corner the gain is laid between them. The size of transistor for cascode OTA is tuned and finallythe total current is about 91µA for cascode which means this OTA uses only 82µW. This brings us a very low power and high performance architecture which can be used freely in the circuit as needed without worrying about its energy consumption. A voltage buffer is used in order to cancel the noise of reference voltage as illustrated in

Figure 4. This buffer should employ high gain OTA to achieve low output impedance and consequently low noise coupling on Vref. High gain in low power and low voltage is very hard and needs consideration of lots of design criteria. This allows the OTA to achieve high gain in lower than 1volte supply voltage. The differential structure of the buffer also tends to increase the offset in the reference voltage as symmetric or random noise[21].

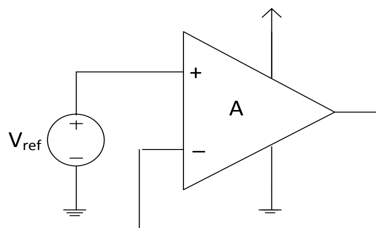


**Figure 4.** Buffer for FinFET based BGR

It's also required that the current initiated from its zero state by a start-up circuit. A typical start-up circuit shown in Figure 5may go to off mode quicker than the circuit's voltages are stabilized. It is of particular concern when the size of the chip and number of the nodes are huge. Therefor some of the block may not start their functionality before the start-up circuit go off.

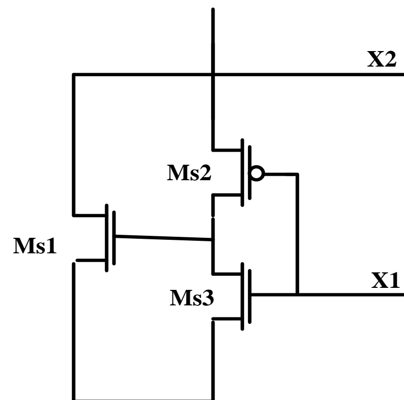


**Figure 5.** Traditional Startup Circuit

## 5CIRCUIT ANALYSIS

In order to finding the temperature coefficient of the reference voltage the resistor assumed to be ideal and the temperature coefficient of diodes voltage, it could be gained that:

$$\partial V_d = -\frac{0.6}{T}$$

Another assumption is the diode junction voltage is about 0.6 in 300˚K.

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$$V_{d2} = 0.6$$
$$V_3 = V_2 \rightarrow$$
$$R_2 = R_3$$
$$\Delta V_d = R_0 I_{c2} \rightarrow$$
$$I_{out} = \frac{V_T \ln(m)}{R_1} + \frac{V_{be1}}{R2}$$
$$\rightarrow$$
$$\frac{\partial V_{ref}}{\partial T} = \frac{\partial}{\partial T}\left(R_4\left(\frac{V_T \ln(m)}{R_1} + \frac{V_{d1}}{R_2}\right)\right) \rightarrow$$

And for minimum sensitivity to temperature in 300˚Kit should be zero.

$$\frac{\partial V_{ref}}{\partial T} = \frac{R_4 Kq\ln(m)}{R_1} - \frac{R_4}{R_2} \times \frac{0.6}{T} = 0$$

By considering the m=100 for BJTs and also R4=2.7K we could find:

$$\frac{R_2}{R_1} = 5$$

For writing the feedback formulathe Rout of M5 should be find, this equation are as:

$$R_{D5} = 1 / g_{m4} \quad (5)$$

So the gain of feedback equal to:

$$A_f = g_{m5} \times R_D \rightarrow A_f = g_{m5} / g_{m4} \quad (6)$$

This equation shows that the gain of feedback is related to the gm ratio of M5 to M4. So with regulate this parameter the circuit canachieve to optimum gain.

## 6SIMULATIONS AND FEATURES OF SELECTED BANDGAP

The gate control of the transistor in FinFET is much higher which reduce the short channel effects (SCE). The higher on-current of transistors and lower than 70mV/dec subthreshold slop in FinFET technology can utilize to have speedy device by lower power consumption.The usage of 32nm transistors makes proposed bandgap very compatible with digital parts of the integrated circuits (IC). This alluring characteristic is magnified through now-a-days ICs design with lower area and power for analog parts. In TT corner the variation of output voltage versus temperature between -40 °C and 120 °C is depicted in

Figure 6. The variation in reference voltage isminimized in TT corner.The temperature dependence of output voltage in different process corners was found and archived in

Table 2. The temperature varied between -40 and 120 for bulk CMOS and FinFET devices respectively. The temperature dependency for long channel FinFET is lower than comparable CMOS transistors.

Table 2–Compare of variation in output voltage between -40 and 120 in all corners for bulk CMOS and FinFETdevices (%)

| CORNER | Variation of output for bulk CMOS (%) | Variation of output for FinFET |
|---|---|---|
| SS | 0.063 | 0.052 |
| SF | 0.038 | 0.032 |
| FS | 0.047 | 0.040 |
| FF | 0.039 | 0.034 |
| TT | 0.041 | 0.035 |

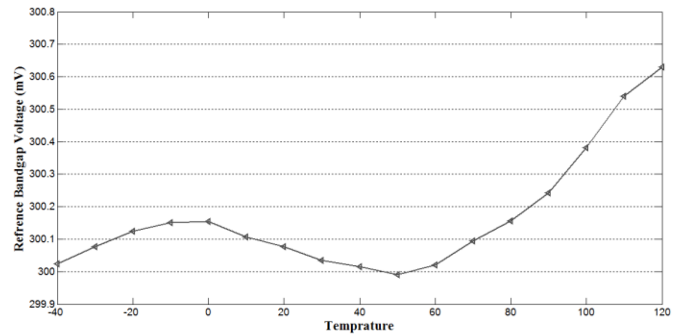


**Figure 6.** variation of reference voltage versus temperature in TT corner (0.041%)

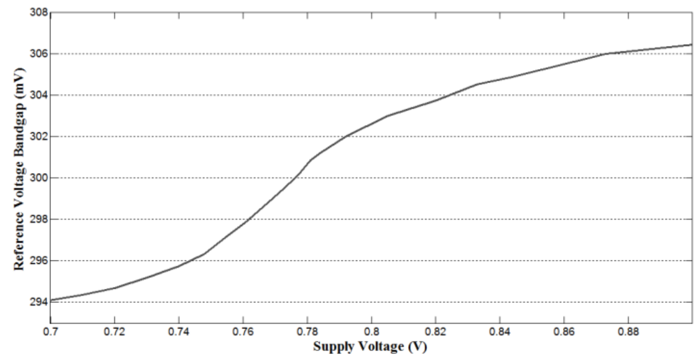


**Figure 7.** Variation of output voltage versus VDD (0.01%)in TT corner

Final tuning was done to achieve the minimum variation in output voltage in all corners. This needs some deviation from the ratio of resistor was found by hand calculation. Then the supply voltage was swept between 10% of its value and the output voltage versus VDD was found as depicted inFigure 7.The variation of reference voltage under such variation is below 0.01%.Finally the circuit was tested under Monte-Carlo simulation to model random mismatch between components which are results of process variation. Applying the different value of VT was done by generating a Gaussian function for each of the parameters. Some data about Gaussian function is needed as follow:

η= the mean value of Threshold voltage
σ2 = the variation of random data

These data applied to the circuit and reference voltage under this data vector was found. Finally the output data was extracted from .lis file's data is used and by a simple programing the numbers of samples of Vref in each interval were found. The different values of Vref for variety of temperature and process corners which are result of variation in threshold voltages. The maximum variation for Vref is as low as 1.45mV which is results of using high gain OTA with Fin-FETs. Indeed using the Non-ideal resistors which are available in the technology in this method make this approach

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very attractive and easy to fab. These numbers which demonstrate the density of Vref in different amplitudes were illustrated in Figure 8.

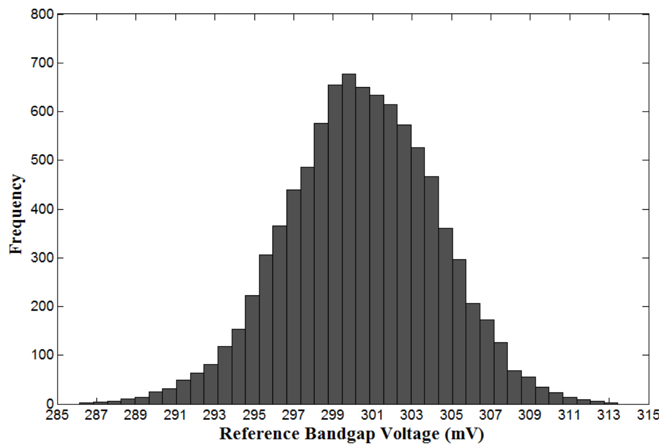


**Figure 8**. Distribution of Vref

The most important factor affecting current symmetry of main BGR circuit and thus the output voltage is the Channel Length Modulation (CLM). The drain-source voltage of the M1-M3 pair transistor is dependent to the temperature severely. An amplifier is used in order to regulate this voltage and keep it in the same value for both transistors. Figure 9 shows the effect of M1-M3 transistors in BGR voltage.

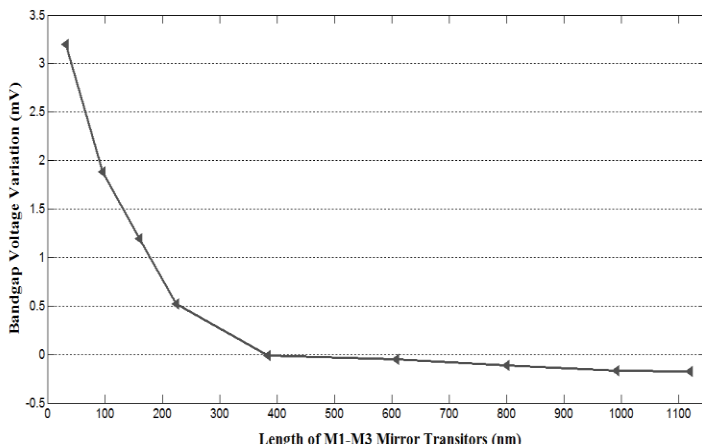


**Figure 9.** Effect of M1-M3 length on voltage bandgap variation

the power Rejection of the circuit from supply voltage is demonstrated inFigure 10. With use of FinFET devices the circuits can achieve more PSRR than bulk CMOS.

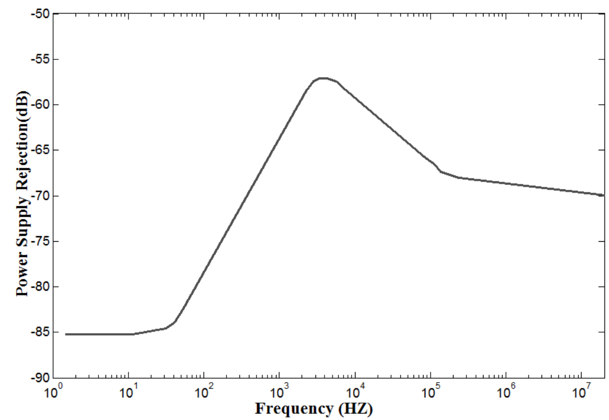


**Figure 10.** Power supply Rejection

## 7 CONCLUSION

In this paper is introduced a new topology of bandgap voltage circuit. This architecture generate stable and regulate output voltage with using of extra feedback. This feedback makes circuit more stable against PVT variation and noise. Use of FinFET devices provide extra pin for controlling threshold voltage of this device bygiving the voltage to back gate of it. BGR is used from the back gate of output Stage as controller of output current.High gain OTA utilized in the feedback loop was designed by innovative bulk FinFET devices which are very low power and high speed compared to conventional CMOS designs . It was tested with supply voltages between 0.7 and 0.9 volt and between -40∘C and +120∘C. this circuit generates a reference voltage of 300mV with only 0.041% and 0.01% variation versus Temperature and VDD variation respectively. 32nm PTM technology is used for simulation

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