Low Voltage Low Power Applications Of 3T Gain Cell

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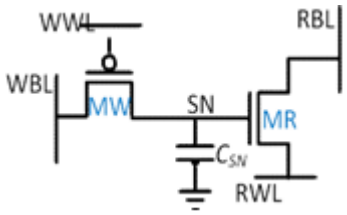
Abstract: Logic compatible gain cell (GC)-embedded DRAM (eDRAM) arrays are considered an alternative to SRAM due to their small size, nonratioed operation, low static leakage, and two-port functionality. However, traditional GC-eDRAM implementations require boosted control signals in order to write full voltage levels to the cell to reduce the refresh rate and shorten access times. These boosted levels require either an extra power supply or on-chip charge pumps, as well as nontrivial level shifting and toleration of high voltage levels. In this brief, we present a novel, logic compatible, 3T GC-eDRAM bitcell that operates with a single-supply voltage and provides superior write capability to the conventional GC structures. The proposed circuit is demonstrated with a 2-kb memory macro that was designed and fabricated in a mature 0.18-µm CMOS process, targeted at low-power, energy-efficient applica-tions. The test array is powered with a single supply of 900 mV, showing a 0.8-ms worst case retention time, a 1.3-ns write-access time, and a 2.4-pW/bit retention power. The proposed topology provides a bitcell area reduction of 43%, as compared with a redrawn 6-transistor SRAM in the same technology, and an overall macro area reduction of 67%including peripherals.

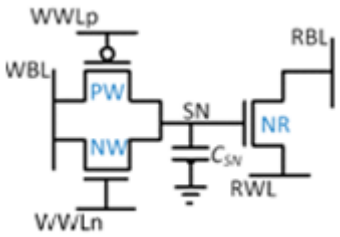
Index Terms: Access speed, data retention time, embeddedDRAM, gain cell, low power operation.

1. INTRODUCTION

In recent years, memories have occupied increasingly large portions of the die area of VLSI systems-on-chip (SoCs), in general, and of microprocessors, in particular, as shown in [1]. This is dueto the large 6-transistor (6T) SRAM bitcell and its area-consuming peripheral circuitry that are the basis for the vast majority of these.In addition, the standby power of ultralow-power (ULP) systems, such as biomedical implants and wireless sensor networks, is often dominated by embedded memories, which continue to leak during the long retentive standby periods that characterize these systems.The 6T SRAM has been the traditional choice for the implementationof embedded memories due to its high-access speed and refresh-free static data retention. However, the 6T bitcell has several drawbacks in modern systems, including its large transistor count, its impeded functionality under voltage scaling, and the aforementioned static leakage currents from the supply voltage (*V*DD) to GND. One of the interesting alternative implementations that addresses these limitations, while continuing to provide full CMOS logic compatibility, is gain-cell (GC)-embedded DRAM (eDRAM), such as the circuit shown in Fig. 1(a) [2]–[5]. Most often consisting of 2-transistor (2T) or 3-transistor (3T), GC-eDRAMs provide areduced silicon footprint, along with inherent two-port functionality,nonratioed circuit operation, and very low static leakage currents from *V*DD to GND. However, as opposed to static memories, such as SRAM, the data retention of GC-eDRAM depends on dynamically stored charge, and thereby requires periodic, power-hungry refresh operations.



(a) 2TmixedGC.



(b) proposed 3T GC

Fig.1*Schematic of conventiona land proposed GCs.*

The data retention time (DRT) of GC-eDRAMs is the timeinterval from writing a data level into the bitcell to the last moment at which one can still correctly read out the stored information. The DRT is primarily limited by the initial charge stored on the internalbitcell capacitance and the leakage currents that degrade the stored voltage level over time. For traditional 2T and 3T cells, the DRT is significantly affected by the initially degraded voltage level corresponding to data 0 or 1, due to the threshold voltage (*VT*) drop across the write transistor [MW in Fig. 1(a)]. In order to address this problem, a boosted write word line (WWL) voltage is usually employed to pass a full swing level to the storage capacitance.However, this requires the generation of a boosted on-chip voltage, which entails substantial overhead [6]. The magnitude of the voltageboost is set not only to overcome the *VT* drop, but

also to achieve short write-access times, which otherwise are typically longer than for 6T SRAM implementations. Furthermore, charge injection (CI)and clock feedthrough (CF) during WWL signal deassertioncausea voltage step at the storage node (SN), resulting in an initially degraded level at the end of a write access [5]. As this undesired coupling even increases with WWL boost magnitude, a clear tradeoffbetween write speed, power, and DRT is introduced [5]. In addition, the level-shifting and toleration of higher than nominal voltagescan be complex, especially when this boosted voltage is a negativeunderdrive voltage, as required by implementations employing a pMOS MW [2], [4]. The propagation of such a negative voltage can easily lead to voltage drops over device terminals that violate the technology limitations.

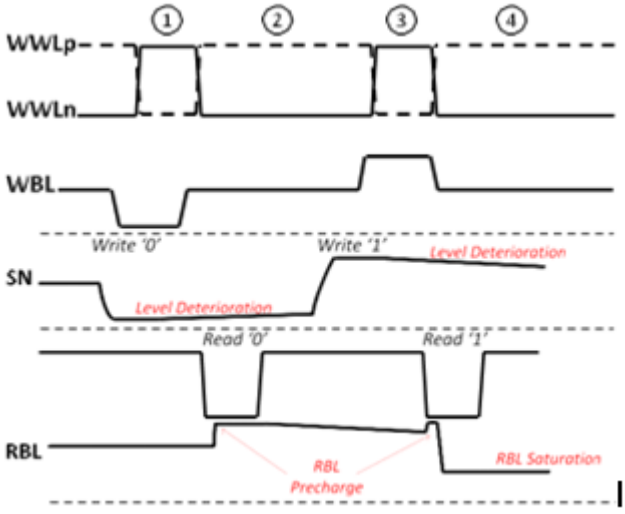


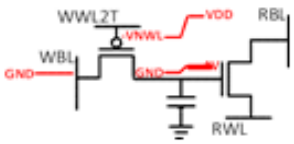
Fig.2.*Timingdiagramofsubsequentwriteandreadoperations. ①Write0.②Readthestored0.③Write1.④Readthestored1. PlotsextractedfromSpectresimulationswithnominalparametervalues.*

Contribution: In this brief, we present a new topology for a 3T GC,featuring a complementary transmission gate (TG) in the write port. While the proposed solution is quite straightforward, to the best of our knowledge, it is novel, and its impact is very high, as shown in this brief. The proposed bitcell provides strong initial data levels (both 1 and 0) for enhanced DRT and robust operation, as well as fast write-access times. This dual advantage is achieved without theneed for additional voltages or boosted signals, allowing the use ofstandard peripheral circuitry for simple SoC integration and small silicon area.In order to demonstrate the functionality of the proposed bitcell, a 2-kb memory macro was designed and fabricated in a mature 0.18-μm CMOS node, which is typically used for ULP applications, such as biomedical sensor nodes and implants. The resulting memory macro consumes only 33% of the area of asingle-port 6T SRAM macro of the same size in the same technology node. The manufactured 3T GC-eDRAM macro is shown to be fully functional with a single-supply voltage ranging from 600 mV to 1.8 V and a worst case DRT of 0.8 ms at 900 mV, resulting in 4.9 nW/2-kb retention power, which is 17× lower than a previously reported6T SRAM at this voltage in the same technology [7].

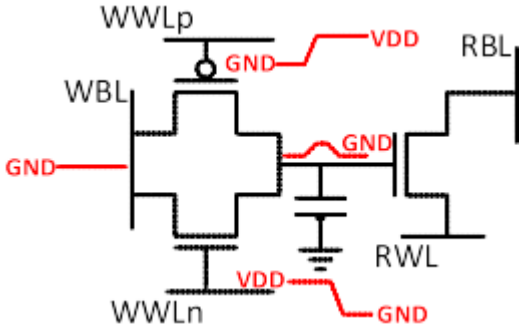
II. PROPOSED 3T GAIN-CELL

A.3T Gain-Cell Structure

Fig. 1(b) shows the schematic of the proposed single-supply3T GC. The circuit comprises a write port featuring a complementary TG PMOS Write (PW) and NMOS Write (NW), a read port based on an nMOS device (NR), and a SN composed of the parasitic capacitance (*CSN*) of the three devices and the stacked metal interconnect.The cell is built exclusively from standard *VT* transistors and is fully compatible with standard digital CMOS technologies.The gates of PW and NW are connected to the complementary word lines, WWLp and WWLn. A common write bit line (WBL) is used to drive data through the TG during write operations. The full-swing passing capability of the TG enables the propagation of strong levels to the SN without the need for a boosted word line. Read is performed by precharging the read bit line (RBL) and subsequently driving the read word line to GND, thereby conditionally discharging the RBL capacitance if the SN is high (data 1) or blocking the discharge path if the SN is low (data 0). To achieve a reasonable tradeoff between speed, area, power, and reliability, a dynamic sense inverter is used on the readout path (Section III-A). However, other sense amplifiers can be used for improved read performance, such as demonstrated in [3], [8], and [9].



(a)



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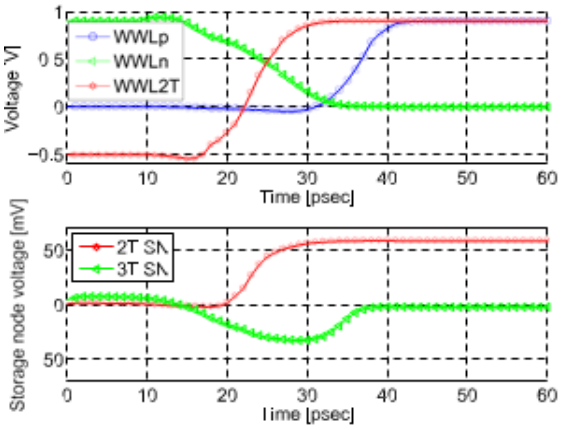


Fig.3.*EffectsofCIandCFmechanisms.(a)Conventional* 2Tbitcell.(b)Proposed3Tbitcell.(c)Waveformcomparisonofth etwobitcellsduringwritedeassertion

B. 3T Gain-Cell Operation

Fig.2 demonstrates bitcell operation through the applicationof subsequent write and read operations of both data valueswith *V*DD = 900 mV. This supply voltage was chosen as a good median voltage between *V*DD and *VT* , as previously shown to be DRT efficient in GC-eDRAM design [5]. Starting with a charged *C*SN (①), WBL is driven low and the word lines are asserted (WWLp= 0 and WWLn= *V*DD). As expected, a strong 0 level is passed to the SN, and this level is retained with the deassertion of the word lines due to the opposing CI and CF effects from the PW and NW transistors. During standby, the level on SN deteriorates due to leakage currents, dominated by the sub-*VT* leakage of NW and PW in mature CMOS nodes. Therefore, in order to extend the retention time,WBL is driven to *V*DD/2 during standby and read cycles, thereby significantly reducing the sub-*VT* leakage through the TG, for both stored data 0 and 1, compared with the case where WBL is driven to either *V*DD or GND. The WBL biasing circuitry is described in Section III-A.During readout (②), the 0 level blocks the discharge paththrough NR, maintaining the precharged voltage on RBL. During the next write operation (③), WBL is driven high, resulting in a strong 1 stored on the SN. The subsequent read operation (④) provides a strong gate overdrive to transistor NR, thereby discharging RBL toread a 1. It should be noted that during this operation (Read 1), bitcells storing 1 and sharing the same column turn on when RBL discharges by more than the *VT* of NR, causing it to saturate before it can completely discharge. This phenomenon is common to many GC-eDRAM configurations, as discussed in [5].

C. Comparison With Other Gain-Cell Implementations

A major advantage of the proposed cell over previous2T and 3T GCs is the self-dampening effect of CI and CF during write, as demonstrated in Fig. 3. For a 2T cell with a pMOS MW [Fig. 3(a)], CI and CF cause a significant positive voltage disturbance

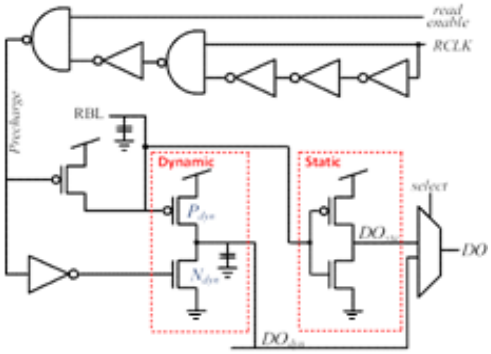


Fig.4.*Dynamicreadoutarchitecture*

on the SN during the rising edge of WWL, resulting in a degradedinitial 0 level. However, in the proposed 3T cell [Fig. 3(b)], this problem is avoided due to the opposite transitions of the complementary WWLs (WWLn and WWLp), and the opposite polarity of charges injected into *C*SN from the pMOS and nMOS MWs. This behavior is plotted in Fig. 3(c) for the two configurations with *V*DD = 900 mV and an underdrivevoltage of −500 mV for the 2T to pass a full 0 level on the falling edge of WWL [5]. Whereas the 2T cell suffers from a degraded level of over 50 mV after WWL deassertion, the CI and CF effects of thecomplementary devices in the 3T cell essentially negate each other, resulting in a strong 0 V level for this cell. Note that there is still a dip in the 3T SN voltage due to the WWLn signal transitioning earlierthan the WWLp signal. This could be avoided with more careful timing control. This strong level leads to advantages in both DRT, as well as read-access time, as the initial data levels are stronger.

III. MEMORY MACRO PERIPHERALS

The single-supply voltage required for the operation of theproposed topology simplifies the implementation of a full memory macro is a significant advantage over other GC-eDRAMs using conventional bitcells, which require the use of level shifters to create the desired boosted or negative (dependent on the type of MWs) voltage supply. However, to further improve the array performance, in terms of access time and power consumption, several peripheral techniques were integrated into the designed memory macro. These peripheral circuits and techniques are presented in the followingsections.

A. Readout Circuitry

Many previous low-voltage embedded memories, targeted atULP systems, employ a simple sense inverter in order to provide robust, low-area, and low-power data readout. However, such an inverter suffers from a very slow readout, as it requires the RBL to be discharged (charged for a pMOSread device) past the switching threshold of the inverter, which is hard to deviate away from *V*DD/2. This operation is further impeded by the aforementioned RBL saturation during readout that slows down the discharging (charging) operation, as the RBL voltage decreases (increases).Therefore, the readout path that was integrated into the proposed 3T GC-eDRAMmacrocell has two sensing modes: 1) a faster, yet potentially more error-prone, dynamic readout mode and 2) a slightly slower, yet more reliable, static mode. In all measured prototype chips, both

the dynamic (preferred for speed)and static modes were tested successfully. In both sensing modes,Low Threshold device (LVT) pMOS transistors were used in order to allow a faster yet accurate read-access time, due to the aforementioned issues. The supply voltage to the readout circuitryis gated with the read enable signal in order to save substantialstatic power due to the leaky LVT devices. The schematicsof the two alternative readout circuits are shown in Fig. 4. The rising edge of the read clock creates a precharge pulse that charges the parasitic capacitance of RBL and discharges the output capacitance of the dynamic sense inverter (DOdyn) through the discharge transistor, *N*dyn. Subsequently, RBL is conditionally discharged during the read operation, turning on *P*dynto flip the output if a 1 is stored in the selected cell. Therefore, an RBL swing of only one *VT* is required to complete a read operation. Transistor sizes for the dynamic sense inverter and pulse generator were chosen according to postlayout simulations under global and local parametric variations.

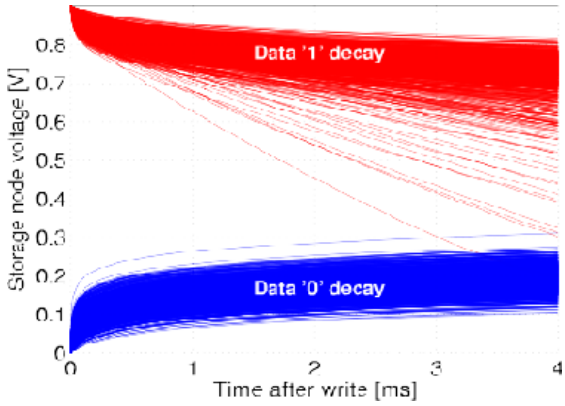
B. Write Circuitry

While the proposed single-supply 3T bitcell provides a significantimprovement in both write time and initial SN level over standard GC implementations, the dual-transistor write port adds an additional leakage path to/from the SN. The increased aggregated sub-*VT* current causes faster degradation of the stored charge, leading to reduced DRT, as compared with a reference 2T cell. In addition, several previous works have shown that the data dependent, asymmetric DRT (for data 0 and 1) of standard GCs can be manipulated to overall enhance DRTs by biasing the WBL at the best case voltage for the weaker data level during standby and read operations [10]. For theproposed 3T configuration, the worst case DRTs of the 1 and 0 levels are similar, and significant deterioration of the stored levels occurs for both extreme values of WBL bias (*V*DD and GND). However,a neutral bias of *V*DD/2 can be applied, thereby greatly reducing the sub-*VT* current through the TG. Fig. 5 shows the benefit of this measure, displaying the level degradation of stored 1 and 0 data with WBL biases of opposite polarity and *V*DD/2. With a WBL bias of *V*DD/2, the DRT can be extended by ~1000×. The write circuitry to implement the median WBL bias duringstandby and read cycles is shown in Fig. 5(c). A standard inverter chain conditionally drives the data-in level on to the WBL through a TG, controlled by complementary write enable signals Write Enable (WE) and Write Enable Negative (WEN). In parallel, a pair of long-channel I/O devices drive WBL during nonwrite cycles. These devices create a short-circuit path between *V*DD and GND when WE is low, providing a median potential (*V*DD/2). at WBL. Due to the thick oxides and long channel-lengths of the I/O devices, process variations are significantly reduced, and the static current is extremely low. Based on the chosen transistor sizes, the static power consumption of the proposed WBL driver during nonwrite cycles is only a few femtowatts under a 900-mV supply voltage, which is negligible compared with the refresh power of the array.

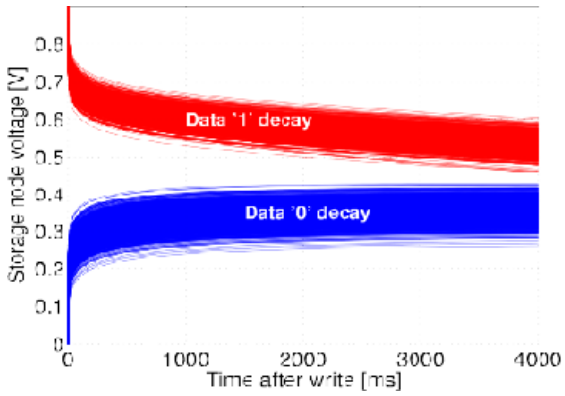
IV. TEST CHIP AND MEASUREMENT RESULTS

A. Implementation and Testing Procedure

A 64×32 bit (2 kb) memory macro based on the proposed 3T GCwas designed in a standard 0.18-*μ*m CMOS process and integrated into a larger test chip with various test structures. All devices were implemented with standard *VT* transistors to provide complete logic process compatibility without the need for additional process steps.Minimum-sized MWs were used in order to achieve a small bitcellarea, while a slightly wider read transistor was employed in order to improve read-access time. The WWLs were routed with horizontal polysiliconstripes to provide a dense bitcell, while other signals wererouted on the first (lowest) three metal layers. Higher interconnect layers (metals 4 and 5) were tightly stacked above the bitcelltoincrease*C*SN.



(a)



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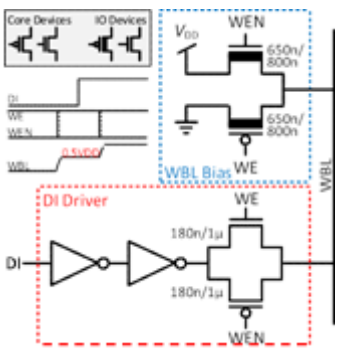
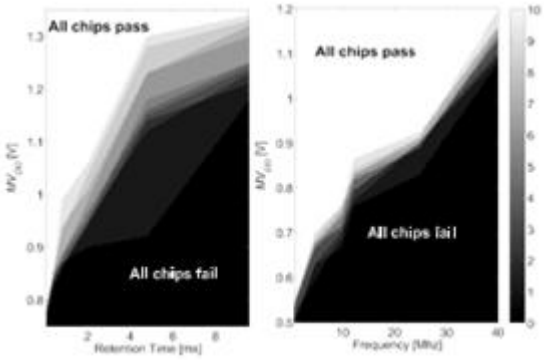


(c)

Fig.5.*Improved DRT through VDD/2 WBLbiasingandtherequiredcircuitry.Plotsinclude1kMonteCarlosamplesat27°Cwith VDD=0.9V.(a)SNdegradationwithworstcasebiasconditions.(b)SNdegradationwithVDD/2WBLbiasing.(c)WritecircuitryforVDD/2biasing*



(a) (b)

Fig.6.*MinimummemorysupplyvoltageShmooplotsfor10measuredchips.(a)MinimumMVDDversusDRT.(b)MinimumMVDDversusfrequency.*

Fig. 6(a) shows a Shmoo plot of MVDD versus the measured DRTfor 10 different chips. The grayscale map corresponds to the number of chips that were fully functional for the respective *V*DD and targeted DRT. The gray levels are a result of global (die-to-die) variations, affecting the DRT of the array for a given MVDD. Even though lowering MVDD results in lower leakage currents from/to the SN, the margin between 1 and 0 levels decreases, resulting in a lower DRT. We note that if this range of DRTs is insufficient previously reported techniques, such as body biasing [11], can be used. The functionality of the memories at different frequencies isshown in Fig. 6(b) for various MVDD voltages, as measured for 10 different chips. The measurement was conducted by writing 1 to all bits of the array and reading them out after the previously measured maximum DRT. The operating frequency was swept for every MVDD to provide the Shmoo plot. The array showed full functionality for all frequencies up to 40 MHz with a supply voltageof 1.2 V. Measurements at higher frequencies were impossible due to limitations of the test setup, which was designed for low-frequency ULP applications. The memory frequency is limited by the read-access time, sinceduring readout, RBL needs to discharge in order to flip the sense inverter. This operation strongly depends on the parasitic capacitance of the RBL, as well as the data held in the unselected cells sharing the same column. If any of these cells stores a 1, the RBL discharge saturates at around *V*DD–*VT* , since at that point the unselected NRs start conducting and counteract the discharging efforts of the selected bit. In addition, due to the fact that readout was performed after the maximum DRT for each *V*DD, a worst case scenario was measured, since the data in the cells was already deteriorated, making the drive current much lower compared with the case where strong data levels are stored in the cells. Raising *V*DD clearly improves the read-access time due to a stronger drive current, which makes the sense inverters switch faster. For a dynamic memory, the relevant metric for static powerconsumption is retention power, composed of the sum of leakage and refresh power. Retention power was measured for storing an entire array of 0 and 1 under supply voltages ranging from 600 mV to1.2 V. Leakage power mainly consists of sub-*VT* currents from theSN to the WBL, which is biased at MVDD/2 during standby periods. The measured retention power was found to be 4.9 nW for MVDD = 900 mV and 1.01 μW for MVDD = 1.2 V, which is 17× lower than a previously reported 6T SRAM cell [7], operated at 1.2 V in the same technology node (consuming 26 μW standby power with *V*DD = 1.8 V). The refresh frequency for every MVDD was selected according to previously measured minimum DRTs.

V. CONCLUSION

This brief proposes a novel 3T GC eDRAMmacrocelltargetedat ULP systems and providing high storage density. The proposed GC is operated from a single-supply voltage, eliminating the need for boosted voltages, commonly found in prior-art implementations.Theproposed cell exhibits faster write-access than conventional GC circuits, while minimizing CI and CF through effects, thereby increasing DRTs and reducing refresh power consumption. The cell area is only 57% of a redrawn 6T SRAM in the same technology, making it a suitable alternative to SRAM for low-power memories.A test-chip containing a 2-kb memory macro based on the proposed 3T GC was fabricated in a mature 0.18-μm CMOS technology and several chips were tested. Measurement results show full functionality at voltages ranging from 600 mv to 1.8 V with retention power as much as 17× lower than a previously reported 6T SRAM in the same technology node.

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