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Survey On Various Works Done In Reducing Static Power In Various SRAM Cells

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ABSTRACT: Memory is the basic need of most of the electronic devices. These memories are mainly designed using CMOS transistors. As we talk about CMOS transistors power, area and speed of each transistor is a major issue of concern. But we know that there is a trade-off between these three factors. Still engineers and researchers are working upon these issues. Issue arises when we switch to lower technologies as within the same die area we have to implant more number of transistors which leads to high chip density and thus high parasitic capacitance. Scaling of transistors is another factor. Thus in this paper we will study about various works done in reducing power dissipation in 5T SRAM cell using different methods in different technologies, a bit compromising in area and speed.

Keywords: CMOS, Chip density, Parasitic capacitance, Scaling, 5T SRAM Cell, Power dissipation, Power reduction.

Introduction

In the present era there is a severe need of low power design in electronic devices. One of these designs is a memory design. The need of low power design is because as per Moore's law "for every 18 months, the die area reduces to half and the number of transistors integrated in the die area doubles". This result in very high chip density which results in high power consumption due to high parasitic capacitance thus generated in a circuit. And from here arises the need of low power VLSI design in an electronic circuitry. Recently, the power density has increased due to combination of higher clock speeds, greater functional integration and smaller process geometries. As a result static power consumption is becoming more dominant. Thus recently the power density has increased due to combination of higher clock speeds, greater functional integration and smaller process geometries. As a result static power consumption is becoming more dominant. This is a challenge for the circuit designers. However, the designers do have a few methods which they can use to reduce this static power consumption. But all of these methods have some drawbacks. In order to achieve lower static power consumption, one has to sacrifice design area and circuit performance. With recent aggressive growth of technology scaling, standby leakage power is increased nearly five times each technology. Memory demand in a particular system is growing due to the need of large data storage. This compelled the designers to lead towards compact memory designs, resulting in higher data storage capacities. It is seen that 5T SRAM are more considerable due to their area compactness and power efficiency compared to any other type of SRAMs. Numbers of researches have been done to reduce the static and dynamic power dissipation within the SRAM cell. Here we will discuss about various works done in power reduction in SRAM cell with 5transistors. There are different techniques for decreasing power consumption in any circuit given by different authors. In this paper, a survey is done on various methods adopted to reduce static power in 5T SRAM cell and other SRAMs. A conventional 5T SRAM cell is designed using DSCH tool is shown in fig.1. SRAM stands for static random access memory. It is a type of semi-conductor memory which uses bi-stable latching circuitry to store single bit. The word static here points that it needs not to be refreshed periodically unlike dynamic random access memory. SRAM exhibits data-remembrance but still it can be called volatile memory as it eventually loses the data when memory is not powered. 5T SRAM cell each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. One additional access transistor serves to control access to a storage cell during read and write operations.

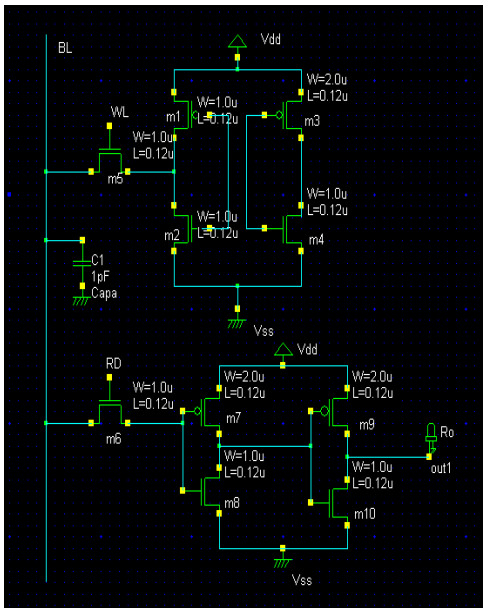

Fig.1. *Schematic diagram of 5T SRAM Cell in DSCH*

Literature Survey

Various types of research works have been done and still going on day by day to increase the reliability of SRAM cell and hence to overcome the tradeoff between area, speed

and power. Few of the research papers have been studied and the work done in that papers are listed below:

Akashe et al (2011) proposed that a 5T SRAM cell with single word line and bit line along with additional read line control. The new cell size was found to be 21.66% smaller than conventional 6T SRAM cell. Delay reduced to 70.15% that of conventional 6T SRAM cell. The power was reduced to 72.10% as compared to 6T SRAM cell. The work was done using Cadence tool in 45nm technology. The proposed 5T SRAM cell is given below.

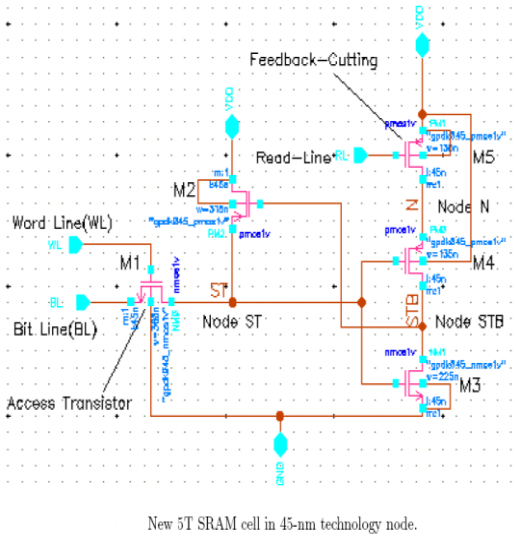

Fig.1. *5T SRAM cell in 45nm technology*

Jain (2011) proposed three techniques i.e. MT-CMOS (Multi- Threshold CMOS), Dynamic Voltage Scaling and Gated Voltage Technique in 90nm CMOS technology using Cadence Virtuoso to reduce leakage power in 6T and 5T SRAM cell. By performing proper read and write operations, leakage current was calculated. Subsequently leakage reduction technique was applied and found that MT-CMOS technique is best. The leakage power in 6T SRAM cell was reduced to 46% and in 5T SRAM cell 43.71%.

Singh et al (2008) proposed a novel 6T SRAM cell for ultra low-voltage applications. Author found 36% improvement as compared to conventional 6T SRAMs. Moving from 130nm to 65nm technology area increased from 71% to 82%. Leakage power was reduced upto 21%. The whole work was done in 65nm technology.

Chetna et al (2012) proposed Dual Vth 5T SRAM cell and compared to dual Vth 6T SRAM cell using 180nm CMOS technology. The leakage current for 5T SRAM cell was found to be 210mu watt and for 6T SRAM cell was found to be 390mu watt. Write delay for “0” and “1” was calculated to be 3.0038e-8ns and 1.53e-8ns respectively for 5T and 3.05e-8ns and 1.51e-8ns respectively for 6T.

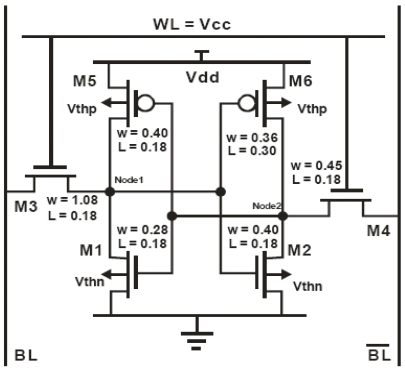

Fig. 2. *Schematic of Dual- Vth 6 T– SRAM Cell with final Size*

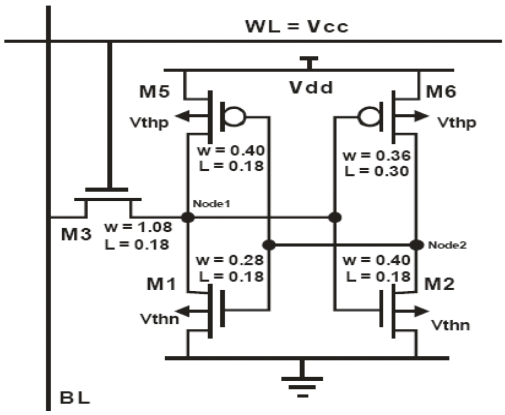

Fig.3. *Schematic Of Dual – Vth 5T- SRAM Cell with final sizes*

Singh et al (2013) proposed a 5T SRAM by using Self Controllable Voltage Level (SVL) technique in which 5T SRAM cell was divided into upper SVL and lower SVL was used. 120nm technology was used with DRC rule checker. The power reduced by this technique was 98%.

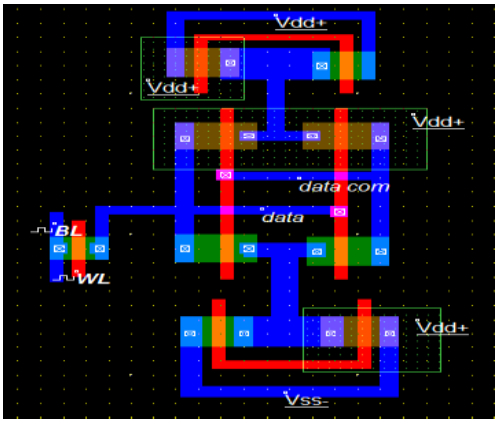

Fig. *Layout of 5T SRAM with SVL Technique*

Birla et al (2010) proposed various circuit design methodologies to reduce leakage power for ultra low power applications. The work was done in 32nm CMOS technology. This method can work for lower technologies till

32nm. The power was reduced up to 4.75% and speed increased to 35.29%.

Gupta et al (2013) reported 7T, 6T, 5T and 4T cells configuration and found the highest stability in 6T SRAM cell. The process was carried out using 32nm technology. The whole circuit verification was done using Tanner tool, design schematic on S-Edit and net list simulation was done using T-spice. Finally, waveforms were analyzed through W-Edit. An asymmetric configuration was implemented to reduce leakage power and found 6T SRAM best. Power dissipation in 6T SRAM cell for standby, reading and writing mode was found to be 8.2e-11, 4.5e-7 and 5.23e-11 respectively. Delay calculated for read and write was 25ns and 0.8ns respectively.

Rani et al (2012) proposed an 8-bit 6T SRAM cell with Low Subthreshold leakage power using leakage current reduction technique. The circuit was designed using 180nm CMOS/ VLSI technology in Micro-wind tool and found 50% less power consumption than conventional 6T SRAM.

Conclusion

Above are the datum found when studied about the work done in various types of SRAM cells and found. The table below lists the performance parameter of the various works mentioned above.

Method	**Technology/ Topology**	**Cell Size**	**Leakage Current Reduction**	**Speed**
-	45nm (6T)	21.66% less than standard 6T Sram Cell	72.10% less than standard 6T SRAM cell	28.57% better
MT-CMOS Technology	90nm (5T & 6T)	-	43.71% in (5T) 46% in (6T)	-
-	180nm (5T)	-	4.75% less than conventional 5T SRAM	35.29% better
SPICE Method	32nm (6T)	-	Power dissipation for read and write calculated 4.5e-7 and 5.23e-11 respectively	25ns read delay, 0.8ns write delay
Dual Vth SRAM cell	180nm (5T & 6T)	-	210muw (5T) & 390mu w (6T)	*
-	65nm (6T)	8% more	21% less	-
Low Subthreshold Leakage Power Reduction	180nm (8-bit, 6T SRAM cell)	-	21% less	-

Note

"**-**" - Not discussed by author

"*****" - Mentioned in literature survey

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