Design And Analysis Of Low Power And High Speed Double Tail Comparator

Madhumathi S, Ramesh Kumar J

M. E Student, Department of ECE, K. S. R College of Engineering, Tiruchengode, Tamilnadu India
Assistant Professor, Department of ECE, K. S. R College of Engineering, Tiruchengode, Tamilnadu India
madhuredmay@gmail.com, rameshatrs@gmail.com

ABSTRACT: A new double tail parallel latch load comparator are compared in term of voltage, power, delay and offset voltage. CMOS dynamic comparator which has dual input, dual output inverter stage suitable for high speed analog-to-digital converters with low voltage and low power. A single tail comparator is replaced with a double tail dynamic comparator which reduces the power and voltage by increasing the speed. The technology scaling of MOS transistors enables low voltage and low power operation which decreases the offset voltage and delay of the comparator. The proposed algorithm replaces some pair of transistors connected in parallel for offset voltage reduction in double tail comparator due to mismatch in transistor pairs. Low voltage and low power consumption are the two most important parameter of the comparator which is to be used in high speed ADCs. 0.25µm CMOS technology confirms the analysis result, frequency=41MHz and given supply voltage will be 0.8v.

Keywords: Double-tail comparator, latch load, offset reduction.

I. INTRODUCTION

COMPARATORS have a crucial influence on the overall performance in high speed analog to digital converters. Due to low-offset, fast speed, low power consumption, high input impedance, CMOS dynamic latched comparator are very attractive for many applications such as high speed analog-to-digital converters (ADCs), memory sense amplifiers (SAs) and data receivers [1]. Scaling is used in CMOS transistor to decrease power consumption and occupying area. Offset-voltage of the comparator exceeds tens mV due to transistor mismatch [2]. They use positive feedback mechanism with one pair of back-to-back cross coupled inverters [3] in order to convert a small input-voltage difference to a full-scale digital level in a short time. However, an input-referred latch offset voltage, resulting from static mismatches such as threshold voltage Vth and β variations in the regenerative latch, deteriorates the accuracy of such comparators. Moreover, dynamic mismatch from the unbalanced parasitic capacitances [3] on the output nodes of the latch causes the additional offset term during evaluation phase. Because of this reason, the input-referred latch offset voltage is one of the most important design parameters of the latched comparator. If large devices are used for the latching stage, a low offset can be achieved at the cost of the reduced speed due to slowing the regeneration time and then increased power dissipation. In this paper we are going to implement the some pair of transistors which is connected in parallel for offset voltage reduction in double tail comparator due to mismatch in transistor pairs. A new technique which uses the latch as load in the first stage is used to reduce offset voltage in the second stage. Fast speed and low power consumption are the two most important parameter of the comparator which is to be used in high speed ADCs. The technology scaling of MOS transistors enables high-speed and low power operation but the offset voltage of the comparator is decreased due to this work. This paper is organized as follow. Section II, describe as double tail comparator reducing a power, delay and section III introduced proposed double tail comparator with latched load cascade and parallel connection for reducing power, delay. In parallel connection delay will reduced compare to cascade. Section IV describes simulation result for previous and proposed method. Section V table comparison for transistor, power, voltage, delay and conclusion is draw in section VI.

II. PREVIOUS WORK CIRCUIT

The double-tail dynamic comparator due to the better performance of double-tail architecture in low-voltage applications, the comparator (Fig.1) is designed based on the double-tail structure. The main idea of the comparator is to increase Δvth/β in order to increase the latch regeneration speed. The operation of the comparator is during reset phase (CLK = 0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD, hence transistor M1c and M2c are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground. During decision-making phase (CLK = VDD, Mtail1, and Mtail2 are on), transistors M3 and M4 turn off. Furthermore, at the beginning of the phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages.

![Double tail dynamic comparator](image)

Figure 2. Double tail dynamic comparator
Suppose $V_{INP} > V_{INN}$, thus $f_n$ drops faster than $f_p$, (since $M_2$ provides more current than $M_1$). As long as $f_n$ continues falling, the corresponding p MOS control transistor ($M_c$ in the case) starts to turn on, pulling $f_p$ node back to the VDD; so another control transistor ($M_c$) remains off, allowing $f_n$ to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which $\Delta V_{fn}/f_p$ is just a function of input transistor transconductance and input voltage difference, in the structure as soon as the comparator detects that for instance node $f_n$ discharges faster, a P MOS transistor ($M_c$) turns on, pulling the other node $f_p$ back to the VDD. Therefore by the time passing, the difference between $f_n$ and $f_p$ ($\Delta V_{fn}/f_p$) increases in an exponential manner, leading to the reduction of latch regeneration time. Despite the effectiveness of the idea, one of the points which should be considered is that in the circuit, when one of the control transistors (e.g., $M_c$) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., $M_c$, $M_1$, and $M_{tail1}$). To overcome the issue, two nMOS switches are used below the input transistors. At the beginning of the decision making phase, both switches are closed and $f_n$ and $f_p$ nodes start to drop with different rates according to input voltage. So as soon as the comparator detects that one of the $f_n$ and $f_p$ nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that $f_p$ is pulling up to the VDD and $f_n$ should be discharged completely, hence the switch in the charging path of $f_p$ will be opened (in order to prevent any current drawn from VDD) but the other switch connected to $f_n$ will be closed to allow the complete discharge of $f_n$ node. In other words, the operation of the control transistors with the switches emulates the operation of the latch.

III. PROPOSED CIRCUIT

Proposed comparator circuit shown in Figure 3 the topology has low voltage, low power and delay will reduced, offset voltage also reduced at common mode voltage (VCM). The operation of the proposed comparator is as follow.

III. SIMULATION RESULT

To compare the performances of the proposed comparator with the previous works, each circuit was designed using 0.25µm CMOS technology, frequency at 41MHz is simulated at Tanner 13 version.
Figure 4. Double-tail dynamic comparator 1

Figure 5. Simulated waveform for comparator 1

Figure 6. Double tail dynamic comparator 2

Figure 7. Simulated waveform for comparator 2

Figure 8. Proposed double tail dynamic comparator 3 with cascade connection
VI. CONCLUSION

In this paper present a various circuit we present a double tail comparator with cascade and parallel connection is proposed. The latch load cascade and parallel connection will reduce an offset voltage due to mismatch the transistor pair, delay will reduced. This proposed comparator will reduce offset, voltage, delay, power and high speed. In parallel connection delay will reduce compare with cascade connection.

REFERENCE


[5]. Shaikmasthanvali,pylarayesh “A 3GHZ low offset fully dynamic latched comparator for high speed and low power ADCs” in international journal of emerging technology and advanced engineering vol.3,issue 6,june 2013,pp.96-102.


