Design And Analysis Of Low Power And High Speed Double Tail Comparator

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ABSTRACT: A new double tail parallel latch load comparator are compared in term of voltage,power,delay and offset voltage.CMOS dynamic comparator which has dual input, dual output inverter stage suitable for high speed analog-to-digital converters with low voltage and low power. A single tail comparator is replaced with a double tail dynamic comparator which reduces the power and voltage by increasing the speed. The technology scaling of MOS transistors enables low voltage and low power operation which decreases the offset voltage and delay of the comparator .The proposed algorithm replaces some pair of transistors connected in parallel for offset voltage reduction in double tail comparator due to mismatch in transistor pairs. Low voltage and low power consumption are the two most important parameter of the comparator which is to be used in high speed ADCs. 0.25µm CMOS technology confirms the analysis result, frequency=41MHz and given supply voltage will be 0.8v.

Keywords: Double-tail comparator,latch load,offset reduction.

I.INTRODUCTION

COMPARATORS have a crucial influence on the overall performance in high speed analog to digital converters. Due to low-offset, fast speed, low power consumption ,high input impedance, CMOS dynamic latched comparator are very attractive for many applications such as high speed analog-to-digital convertors(ADCs), memory sense amplifiers(SAs) and data receivers[1]. Scaling is used in CMOS transistor to decrease power consumption and occupying area. Offset-voltage of the comparator exceeds tens mV due to transistor mismatch [2].They use positive feedback mechanism with one pair of back-to-back cross coupled inverters [3] in order to converta small input-voltage difference to a full-scale digital level in a short time. However, an input-referred latch offset voltage, resulting from static mismatches such as threshold voltage Vth and *ß* variations in the regenerative latch, deteriorates the accuracy of such comparators. Moreover, dynamic mismatch from the unbalanced parasitic capacitances [3] on the output nodes of the latch causes the additional offset term during evaluation phase. Because of this reason, the input-referred latch offset voltage is one of the most important design parameters of the latched comparator. If large devices are used for the latching stage, a low offset can be achieved at the cost of the reduced speed due to slowing the regeneration time and theincreased power dissipation. In this paper we are going to implement the some pair of transistors which is connected in parallel for offset voltage reduction indouble tail comparator due to mismatch in transistor pairs. A new technique which uses the latch as load in the first stage is used to reduce offset voltage in the second stage. Fast speed and low power consumption are the two most important parameter of the comparator which is to be used in high speed ADCs. The technology scaling of MOS transistors enables high-speed and low power operation but the offset voltage of the comparator is decreased due to this work. This paper is organized as follow. Section II, describe as double tail comparatorreducing a power, delay and section III introduced proposed double tail comparator with latched load cascade and parallel connection for reducing power, delay. In parallel connection delay will reduced compare to cascade. Section IV describes simulation result for previous and proposed method. Section V table comparison for transistor, power, voltage, delay and conclusion is draw in section VI.

II PEVIOUS WORK CIRCUIT

The double-tail dynamic comparator due to the better performance of double-tail architecture in low-voltage applications, the comparator (Fig.1) is designed based on the double-tail structure. The main idea of the comparator is to increase $\Delta_{Vfn/fp}$ in order to increase the latch regeneration speed. The operation of the comparator is during reset phase (CLK = 0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground. During decision-making phase (CLK = VDD, Mtail1, and Mtail2 are on), transistors M3 and M4 turn off. Furthermore, at the beginning of the phase, the control transistors are still off (since fn and fp are aboutVDD). Thus, fn and fp start to drop with different rates according to the input voltages.

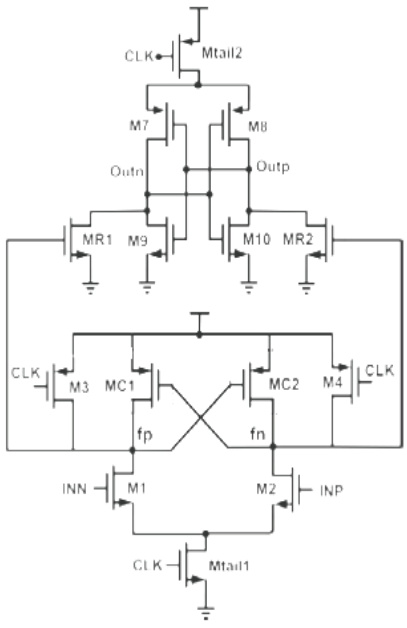

Figure 2. Double tail dynamic comparator

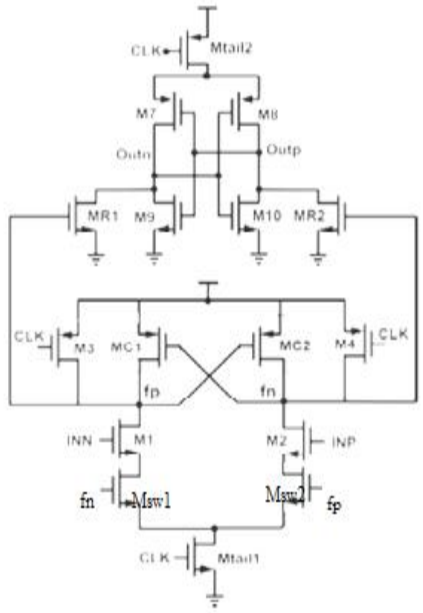

Figure 1. Double tail dynamic comparator 1

Suppose VINP > VINN, thus fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding p MOS control transistor (Mc1 in the case) starts to turn on, pulling fp node back to the VDD; so another control transistor (Mc2) remains off, allowing fn to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which ΔVfn/fp is just a function of inputtransistor trans conductance and input voltage difference, in the structure as soon as the comparator detects that for instance node fn discharges faster, a PMOS transistor (Mc1) turns on, pulling the other node fp back to the VDD. Therefore by the time passing, the difference between fn and fp (ΔVfn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time. Despite the effectiveness of the idea, one of the points which should be considered is that in the circuit, when one of the control transistors (e.g., Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc1, M1, and Mtail1), To overcome the issue, (Fig 2.)two nMOS switches are used below the input transistors [Msw1 and Msw2]. At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to VDD (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the VDD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from VDD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch.

III.PROPOSED CIRCUIT

Proposed comparator circuit shown in Figure 3 the topology has low voltage, low power and delay will reduced, offset voltage also reduced at common mode voltage(VCM).The operation of the proposed comparator is as follow.

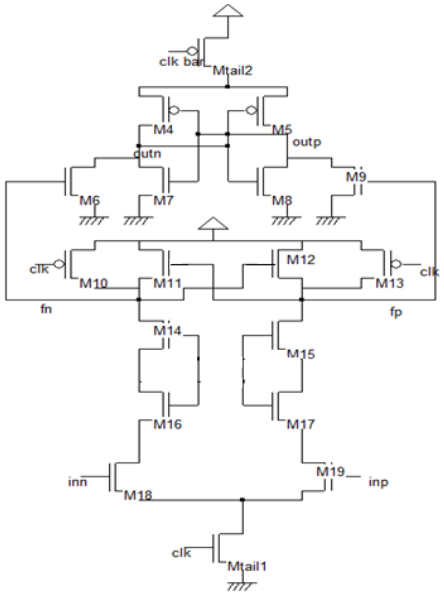

Figure 3. Proposed comparator

During reset phase clk=0, Mtail1 (M3) &Mtail2 (M20) are OFF, M10&M13 will pull both fn&fp nodes to VDD. Hence MC(M11)&MC(M12) are cutoff,M6&M9 are discharge to output nodes to VSS.During an decision making phase clk=VDD,Mtail1(M3)&Mtail2(M20) are ON, transistor M10&M13 will OFF and fn&fp nodes are start drop with different rates according to input voltage. VINP>VINN means fn is faster than fp, M15 transistor provide more current thanM14.MC (M11) is turn On, fp node pulling back to VDD MC(M12) remains OFF, fn node discharged. Adding transistor parallel at proposed circuit. Offset will low and delay reduced. Parallel connected dynamic latch is used as load of first stage to increase voltage difference due to cascade connection delay will more compare to parallel connection.The latch of the first stage start regenerating depending on the input differential voltage (Vin1 – Vin2), producing a large difference voltage. This difference voltage is sense at the second stage input and the second stage latch regenerate output voltage Out1 and Out2.As fast sensing it is exploiting less time to produce output when compare to previous work.It consumes less power compared to conventional one. As the way delay has reduced.

IV. SIMULATION RESULT

To compare the performances of the proposedcomparator with the previous works, each circuit was designed using 0.25µm CMOS technology, frequency at 41MHZ is simulated at Tanner 13version.

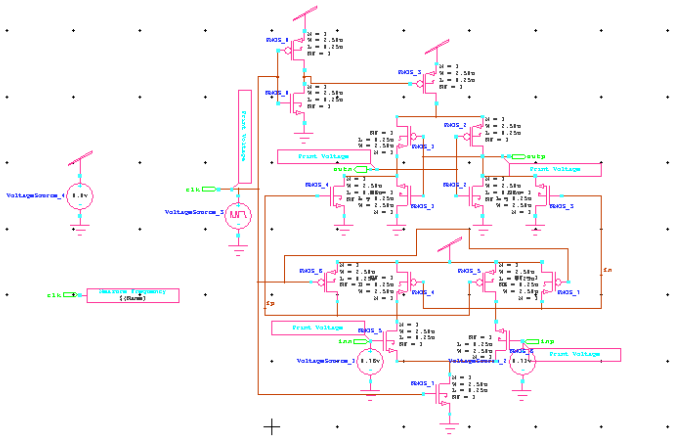

Figure 4. Double-tail dynamic comparator 1

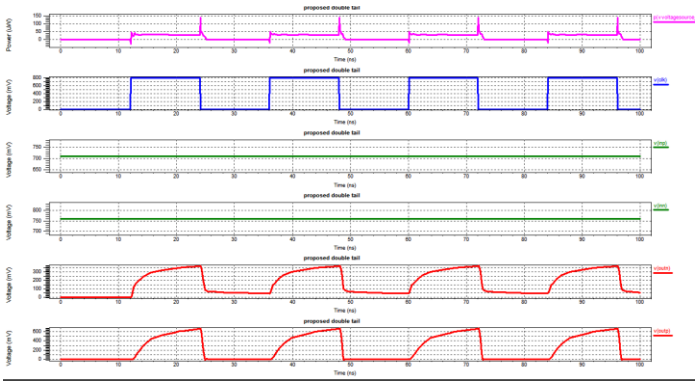

Figure 5. Simulated waveform for comparator 1

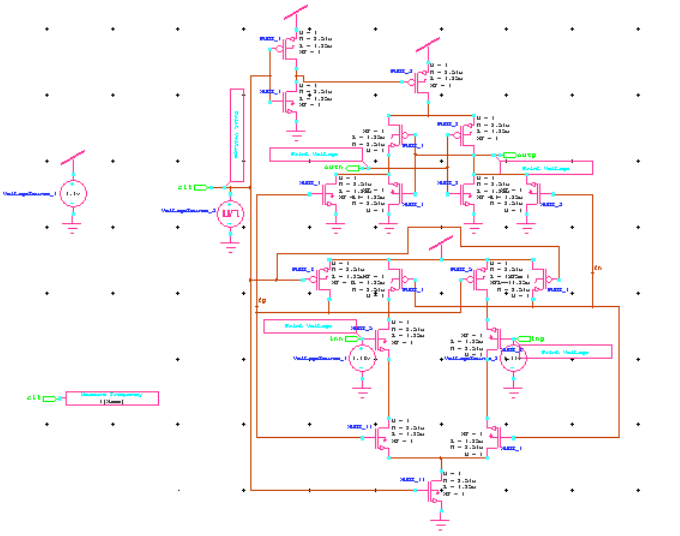

Figure 6.double tail dynamic comparator 2

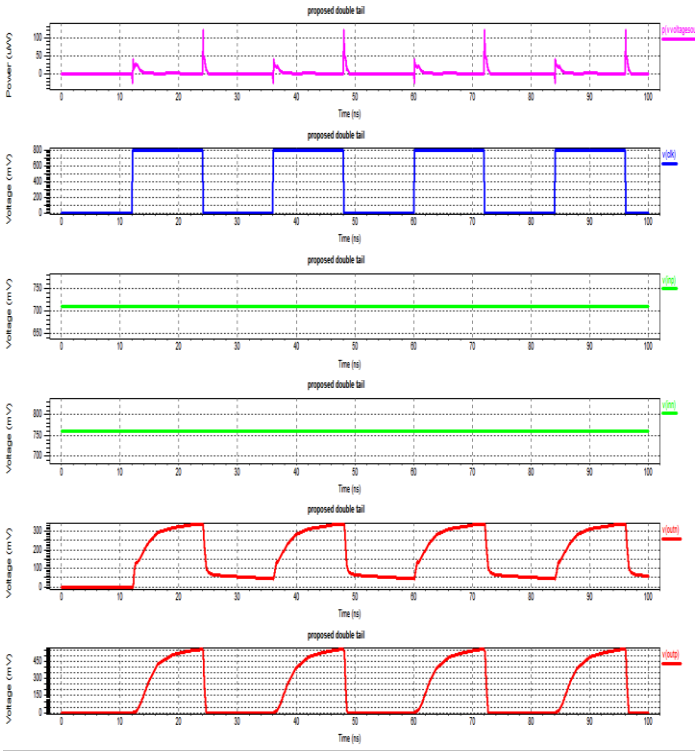

Figure 7. Simulated waveform for comparator 2

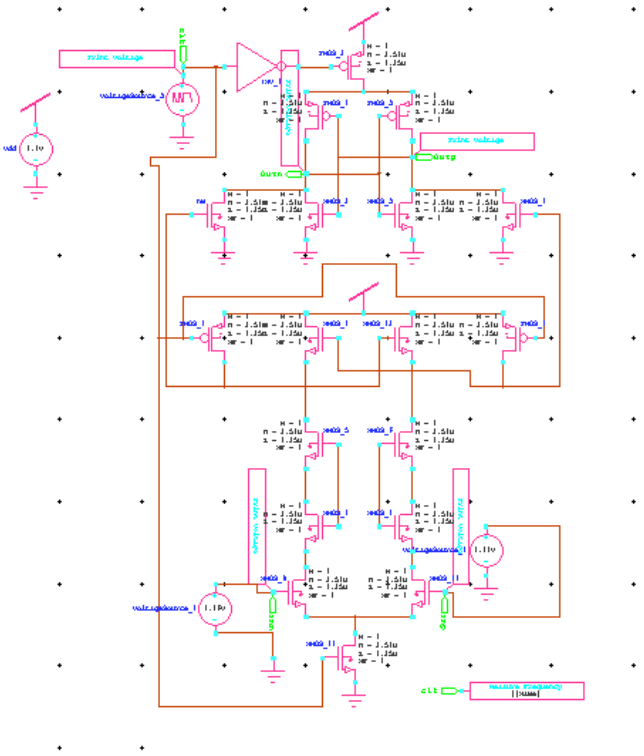

Figure 8. proposed double tail dynamic comparator 3 with cascade connection

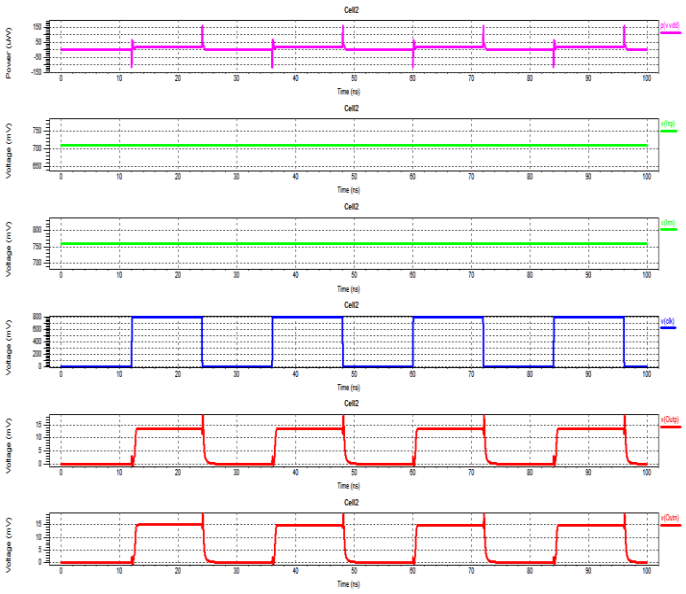

Figure 9. Simulated waveform for comparator 3

V.PERFORMANCE COMPARATION

TABLE-I
NUMBER OF TRANSISTOR ON EACH COMPARATOR

CIRCUITS	NUMBER OF TRANSISTOR
DOUBLE TAIL DYNAMIC COMPARATOR 1	16
DOUBLE TAIL DYNAMIC COMPARATOR 2	18
PROPOSED COMPARATOR 3 WITH CASCODE	20

TABLE-II
VOLTAGE, POWER, DELAY COMPARISION

CIRCUITS	VOLTAGE (V)	POWER (µW)	DELAY (ms)
DOUBLE TAIL DYNAMIC COMPARATOR 1	0.8	16.484	239
DOUBLE TAIL DYNAMIC COMPARATOR 2	0.8	3.721	199
PROPOSED COMPARATOR 3 WITH CASCODE	0.8	9.763	7.217
PROPOSED COMPARATOR 4 WITH PARALLEL CONNECTION	0.8	9.777	6.645

VI. CONCLUSION

In this paper present a various circuit we present a double tail comparator with cascode and parallel connection is proposed. The latch load cascade and parallel connection will reduce an offset voltage due to mismatch the transistor pair, delay will reduced. This proposed comparator will reduce offset, voltage, delay, power and high speed. In parallel connection delay will reduce compare with cascade connection.

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