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Asynchronous Logic Platform with Dynamic Leakage Control using Null Convention Logic

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Abstract: Introducing a method of designing an Asynchronous logic platform with dynamic leakage control by finding a fixed threshold that optimizes both performance and static power will become increasingly difficult into the future. Asynchronous machine architecture will be developed and simulated in Verilog HDL, built using gate models derived from an advanced TBSOI process (STMicro, UTSOI, 28nm). The power and performance characteristics of the platform across a number of applications (drawn from the set of streaming signal processing systems relevant to portable and embedded systems) will be explored along with the potential optimizations available to match the platform to the specific workload under consideration.

Keywords: asynchronous logic platform, dynamic leakage control, NCL

1. INTRODUCTION

The semiconductor industry has long known that it faces a "perfect storm" of technical challenges [1], including excessive power consumption per unit area [2], [3] (especially in portable and embedded systems [4]), the increasing dominance of connecting wires in circuit delays, a greater spread of transistor characteristics, and extreme difficulties with synchronous timing closure and clock distribution [5]. To address this problem requires flexible logic platforms that can reliably deliver high performance at low power and with low cost of design [6]. Although many asynchronous techniques (e.g. [7]) have been proposed eliminate global clocks, none have been commercially successful to date. Null Convention Logic [8, 9], originally developed by Theseus Logic (USA), adds the control value NULL (i.e., not valid) to the Boolean domain to create a symbolically complete and delay insensitive three-value logic system. A gate will only assert its output data when a complete set of (valid) data values is present at its input, thereby enforcing a "completeness of input" criterion. Thus NCL represents a convenient format in which to express asynchronous digital logic. Across a range of embedded computer applications, especially those for mobile and hand–held devices, a tension exists between high performance and low power consumption. To constrain power, we would like to reduce supply voltage but this will reduce the maximum operating frequency. To increase performance, we need to reduce threshold voltage at the cost of an increase in standby (subthreshold) power loss. Finding a fixed threshold that optimizes both performance and static power will become increasingly difficult into the future.

II. METHODOLOGY

In [10], a method was proposed to resolve this tension by allowing thresholds to be dynamically adjusted at run–time using thin–body double–gate Silicon on Insulator (TBDGSOI) transistors. A simple RISC architecture was created using double-gate transistor models and various sub-units of the machine set in either a high threshold (low–leakage) or low threshold (high–leakage) mode by altering the value of their back–gate voltages under the control of the instruction decoder. In this way, only the parts of the machine actually participating in a given instruction would be operating in high-speed mode. This paper seeks to extend that work by applying the technique and analyzing its impact on an asynchronous machine built using NCL technology.

A. NCL technology:

NULL Convention Logic™ (NCL™) is a symbolically complete logic which expresses process completely in terms of the logic itself and inherently and conveniently expresses asynchronous digital circuits. The traditional form of Boolean logic is not symbolically complete in the sense that it requires the participation of a fundamentally different form of expression, time in the form of the clock, which has to be very carefully coordinated with the logic part of the expression to completely and effectively express a process. NULL conventio Logic™ [10] is derived directly from the Invocation Model of Process Expression. The Invocation Model is a conceptual model of general process expression in contrast to a model of computation. It transcends limiting mathematical notions of computation to provide a unifying conceptual framework which relates all forms of process expression from the simplest physical and chemical processes to the most complex natural and artificial processes.

B. Asynchronous Design Using NULL Convention Logic:

Digital circuits designed using asynchronous logic have advantages over clocked designs such as:

- No clock skew
- Lower power consumption
- Lower noise and EMI problems
- No global timing issues
- Better performance in extreme temperatures
- Designing asynchronous circuits can be challenging but the advantanges cannot be ignored

C. Structures of Asynchronous Registers

The interaction behavior among combinational circuits can be seen with the simple pipeline example shown in fig.1

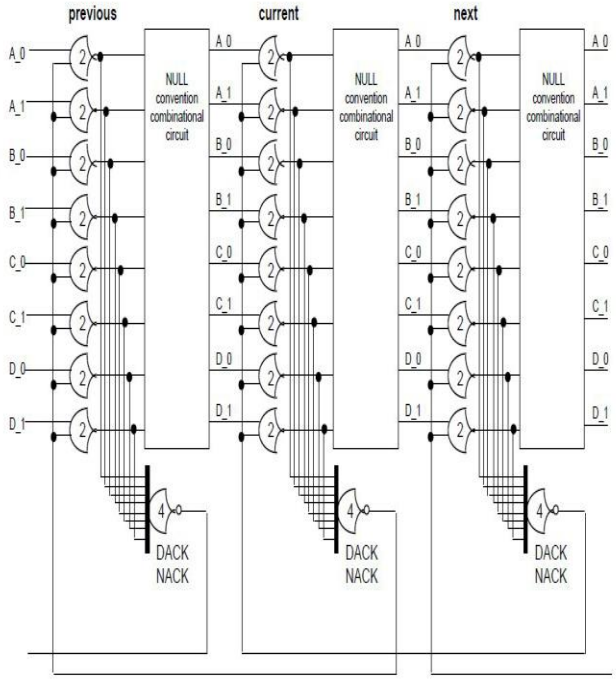

Figure 1. *NULL Convention asynchronous pipeline.*

III. THE 28nm PROCESS FAMILY

The 28nm generation represents TSMC's most energy-efficient and high-performance method of manufacturing to date. 28nm is the first generation that foundry industry starts to use high-K metal gate (HKMG) process. Still, poly/oxynitride process is offered to meet customer's time-to-market need. TSMC's 28nm technology delivers twice the gate density of the 40nm process and also features an SRAM cell size shrink of 50%. The low power (LP) process is the first available 28nm technology. It is ideal for low standby power applications such as cellular baseband. The 28LP process boasts a 20 percent speed improved over the 40LP process at the same leakage/gate. The 28nm high performance (HP) process is the first option to use high-k metal gate process technology. Featuring superior speed and performance, the 28HP process targets CPU, GPU, FPGA, PC, networking, and consumer electronics applications. The 28HP process supports a 45 percent speed improvement over the 40G process at the same leakage/gate.

IV. DESIGN PROCESS

Thus in this work, an asynchronous machine architecture will be developed and simulated in Verilog HDL, built using gate models derived from an advanced TBSOI process (STMicro, UTSOI, 28nm). The power and performance characteristics of the platform across a number of applications (drawn from the set of streaming signal processing systems relevant to portable and embedded systems) will be explored along with the potential optimizations available to match the platform to the specific workload under consideration. A brief idea is shown in fig.2.

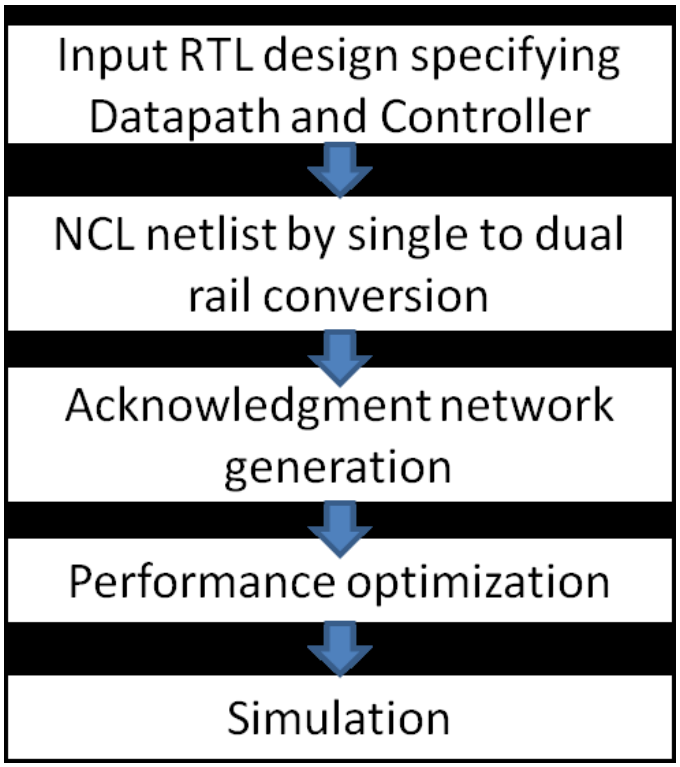

Figure 2. *Design process of asynchronous circuit using NCL logic.*

IV.I. Preliminary Model building:

Performed the development of the primary platform model and specification of appropriate tool flows,. Implemented the NCL asynchronous design from high-level design language (HDL) entry to layout using commercially available tools.

IV. II. Applications design and evaluation:

Performed direct Power/Performance comparisons with platform model and FPGA across a number of applications using a number of standard benchmarks. Useed commercial CAD tools for different stages of the design flow. A synchronous version is also built up for comparing the asynchronous design with synchronous one.

IV. III. Platform Optimization:

The characteristics of the platform are determined under the various workloads presented by these applications, which then allow its architectural reorganization to support optimal performance. The accompanying toolflow is also be optimized.

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