Opto-Electronics Packaging And Failure Analysis Methodology

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ABSTRACT: The demand for opto-electronics is increasing as we are nearing the future due to the need for high data rate, high bandwidth, lossless transmission and low electromagnetic interference sensitivity. The paper describes the present research carried on the mature laser technology i.e. GaAs, in order to improve its efficiency. The packaging principle used for receivers can be applied for the packaging of the laser driver circuit and the laser source in a single module. The concept of FRACAS (Failure Reporting, Analysis and Corrective Action System) has been described and failure analysis technique for Electrical overstress (EOS) is described. An industrial approach to calculating the reliability of a system with some known data facts has been described. Some challenges with respect to packaging have been discussed in detail and some methods to overcome challenges such as lattice mismatch have been described.

Keywords: opto-electronics, opto-electronics packaging, failure analysis, Electrical overstress, Laser driver Packaging, Wirebond

1. INTRODUCTION

Before an electronic product is made available or is designed, an exhaustive survey for the product need and its demand in the market is taken up. Based on this analysis, a team of engineers start identifying the stages of development and these developments happen in parallel. Design of Opto-electronic packaging involves Photonics, Electronics, Mechanical, Thermal, and Vibration engineering. It is also influenced by its operational environment. Test procedures are also required to test and verify electronics package designs and prevent any safety-threatening failures. Hence, analysis of any commercial electronics package before mass production is mandatory.

2. RECOMMENDATIONS FOR OPTO-ELECTRONICS PACKAGING DESIGN

Packaging is nothing but a sequence of process steps involving connecting, protecting and manufacturing of the devices. The widespread commercial use of semiconductor lasers has now included the opportunities to make use array of diode lasers as monolithic components on the Silicon Integrated Circuits (IC's). Presently the laser manufacturers are optimizing the design and process to maximize the laser performance for In GaAsP wafers producing around 10,000 lasers per square inch of the wafer for a compact opto-electronics module packaging. Receivers have been developed which consists of an array of photodiodes along with pre-amplifiers in one module mounted on silicon substrate in one single package, where one side of the photodiode's receive photons and convert it into the desired current or voltage, while on the other side it has electrical contacts in order to trigger the desired component or IC, therefore the same packaging principle can be applied for the array of transmitting lasers that improves manufacturability reducing cost, which has been demonstrated in [6]. Another important aspect of Opto-electronic packaging is the wire bonding. Many Opto-electronics packaging is designed as “butterfly” shape which deals with both electrical and optical signals. The Electrical interconnections are from the cantilever leads to the pads of the die mounted inside the package, where the height difference between the cantilever leads and the die pads are large, therefore it requires the wire bonds to have the capability of deeper access and typically wire bonding in opto-electronic packaging has the first bond on the cantilever leads and the second bond on the die pads due to the bond pads on the cantilever leads being very close to the package walls, therefore to avoid interference of the wedge with the package walls the first bond is normally placed on the leads, and there are three wirebond technologies that are used for opto-electronics packaging i.e. thermo-compression bonding, thermo-sonic bonding and ultrasonic bonding as illustrated in [jianbio pan 2004]. The ability to faithfully reproduce designed features on a wafer is important to the success of optical devices. Critical Dimension (CD) control and smooth device surfaces are two of the most important parameters that must be controlled during processing. Resolving CDs of approximately 350 nm is hardly a challenge for modern optical lithography processes, whose minimum features have already been demonstrated below 45 nm. Resolution, however, is not the only concern when designing planar optical circuits. The need for better resolution demands flat surfaces on which to pattern features. This requirement comes about as a result of the usable Depth of Focus (DOF) at the image plane of standard projection optics lithography equipment; 90 nm process technology has a usable DOF < 300 nm. As a result, wafer topography must be kept below the DOF value to successfully resolve minimum feature size.

3. RECOMMENDATIONS FOR FAILURE ANALYSIS TECHNIQUE

Every product or a system has modes of failure. It is important and necessary to understand why a failure has occurred or why a component has failed in order to rectify the failure and this process is known as FRACAS (Failure Reporting, Analysis and Corrective Action System) [1]. A common failure fault that is encountered during electrical testing is the components damage in a system that is caused due to electrical overstress. Electrical Over-Stress (EOS) is a term used to describe the thermal damage that may occur when an electronic device is subjected to a current or voltage that is beyond the specification limits of the device. During the testing the Voltage v/s Current (VI) characteristics curve is drawn or traced for the input to each components present in the system in order to identify if there’s any electrical input overstress have occurred. The identified failed parts VI characteristics can be compared to the VI characteristics of the good part and if there’s any deviation from the desired response, then the test results are noted and recorded for later examination of that failed part in order to rectify the fault. In industries, all systems that are de-
developed have to undergo environmental tests, mechanical tests and electrical tests in order to detect faults, analyze and rectify them, these test procedures have been illustrated in [10]. Another common technique apart from weibull distribution and exponential distribution model illustrated in [13], is the reliability prediction of a system, where the failure rate of the components and the reliability of the system is calculated. Let’s Assume that 600 parts where stressed at 150°C ambient for 3000 hours with one failure at 2000 hours for a photo resist flaw (0.7eV) and one failure at 3000 hours for an oxide defect (0.3eV); the internal temperature rise (Tj) of the part is 20°C and the product was tested at 1000, 2000 and 3000 hours. Then to find the FIT rate for the process with M=6.3 (chi factor distribution for DOF = 2r+2 for r=2) at 55°C, it is necessary to calculate the Acceleration factors AFs and AFb due to the faults and then the Total Device Hours is calculated followed by the calculation of systems Failure rate in FIT and then the life time of the product or system as illustrated in detail [9]. These predictions are used to evaluate design feasibility, compare design alternatives, identify potential failure areas, trade-off system design factors, and track reliability improvement.

4. CRITICAL DISCUSSION ON PACKAGING DESIGN AND FAILURE ANALYSIS TECHNIQUES

In photonics, one of the limitations is the lack of monolithic long lived laser on silicon, therefore from several years the main effort has been focused on the growth GaAs on silicon; with associated problems related 4% lattice mismatch the two materials i.e. GaAs and Silicon. GaAs or InP compounds exhibit a larger lattice constant than that of Si. The only exception is GaP, which has an indirect bandgap and is not suitable as a laser material. Therefore one of the major roadblocks for further development of optoelectronics with respect to materials is the lattice mismatch between two materials or between the films and the available substrates. Mismatched lattice leads to a high defect density (in the 10^10 - 10^11 level). In spite of the intense efforts made to address this problem, it may not be feasible to reduce the defect density by several orders of magnitude in the conventional approach, until lattice matched substrates are available. Another issue that can be encountered during packaging for optoelectronics is due to the growing density of functionalities and complexity of interfacing inter-disciplinary functions that needs to be integrated in a single system i.e. mechanical, electronics and optics. Proper packaging considering thermal issues, vibrations and shock analysis will lead to a mechanical structure for opto-electronics that is highly reliable and whose survival rate will be longer, thus making the system more reliable. Integration problems related to chemical contamination are likely to pose practical problems due to physical limitations caused due to issues like corrosion. Most conflicts can be addressed by incorporating extra de-contamination steps or adding dedicated tools for the problematic operations, but these solutions can lead to increase in cost. Problems due to chemical contamination have been brought under control in standard silicon processing, but would need to be checked on if the process demands the inclusion of elements and compounds not used in standard processing, but even after its introduction over four years ago, the semiconductor industry is still trying to rectify issues associated with copper (Cu) contamination. There are still no universally acceptable levels of Cu contamination, and many questions still remain about how far beyond the fabrication tools and chambers one must de-contaminate, therefore similar logistical problems may be waiting for the monolithic integration of optical devices with electronics and its packaging.

5. ESSENTIAL MODIFICATIONS FOR THE IMPROVEMENT IN THE SYSTEM

The system design can be improved by making an effort to overcome the problem of lattice mismatch between the GaAs and the Silicon substrate by making use of the available alloys. Optimization of electronic or optical devices require the capability of forming alloys and heterogeneous structures that can provide improvement in lattice matching. Therefore alloys were developed and examined by making use of Nitride compounds such as GaAlN, GaInN. The combination of a mature technology such as GaAs along with GaN to form GaAsN will allow producing light emitting alloys with a wider and better range of lattice constant [2]. Thermal budget limits are critical when integrating different devices into the same process. Failing to account for thermal budgets could result in the inter-diffusion of dopant species, weakening of metal layers, and the introduction of stress due to differing coefficients of thermal expansion. Thermal budgets for both aluminum and copper back-end processes with oxide-based dielectrics are limited by the metal and Interlayer Dielectric (ILD). Although some low-k dielectrics (k < 3.9) are being used (e.g. Carbon-Doped Oxide (CDO)), the thermal stresses and the weaker mechanical properties of CDO will not be able to tolerate temperatures in excess of 450°C; low-k solutions such as Spin-on- Dielectrics will drive the thermal budgets even lower. In the case of electro-optical (EO) polymers, the thermal budget can decrease dramatically, since typical glass transition temperatures are in the range of 150°C - 250°C. For all practical purposes, these polymers can only be integrated as the last steps of the process. The 12 channel 3.125 Gb/s VCSEL laser driver IC has been designed using SiGe BiCMOS process technology. This miniature laser driver IC can be used for development of opto-electronic systems. The driver IC is integrated in a module with an array of 12 VCSEL laser sources. This driver IC’s results has been measured and evaluated [4].

6. CONCLUSION

The laser manufactures are doing optimizations for the laser technology and its performance. Principle packaging for receivers can be applied for packaging of laser driver circuit with laser sources. An important aspect of optoelectronics packaging is wire bond. A basic methodology for failure analysis is the FRACAS. An industrial approach for calculating the reliability of the system is done using the formulas of acceleration factor, failure rate and concept of MTTF. EOS can be detected by plotting VI curve for the input of each component and comparing it to a good known reference curves. An important limitation of the laser source packaging for optoelectronics as the lattice mismatch constant for which alloys are developed using nitrate compounds for better lattice matching of the materials. A laser driver IC is integrated with array of 12 VCSEL laser sources using the BiCMOS process technology which can be packaged into one single miniature module that can be used for the development of optoelectronic system.
REFERENCES


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