High Performance Adder Circuit In Vlsi System

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ABSTRACT: In VLSI system. The integrated circuit design has important role. The various parameters are considering for design the circuit. The important parameters are power and delay. The different tools are used to perform the operation. However, here the combinational circuit (i.e. adder) designed by using different logic. The domino logic is the base of the proposed method. PMOS pull up network (PMOS PUN) is used to perform the operation. The proposed method includes the tradeoff of the power and delay. It designed by using tanner EDA Tool with 1V power supply and 0.5MHz frequency.

Keywords: Domino logic, Power, Delay, PMOS PUN, Integrated circuit.

1. INTRODUCTION

As the need of high speed circuit increases the delay and power consumption problem that can constraint the system performance becomes more critical. Mostly the modern digital CMOS designs are always a great notice for designers to estimate delays and size of logic gates throughout the design phase. In some cases, the designer offers some variations to improve the speed of the circuit. But, these variations give higher power dissipation and area due to the larger gate size. Sizing of transistor is essentially used for minimize the delay, area and power consumption. Another problem of high speed circuit performance is marked by the major component by way of glitches. The static, dynamic domino logics are mainly operated for design the CMOS logic circuits. The domino logic is generally used for avoiding the Glitches. The static CMOS logic [1] is important in the circuit design but the power consumption is high in the static CMOS logic because using equal number of NMOS and PMOS. However, dynamic domino logic [2] overcomes the static logic with minimum area. The dynamic domino logic performed by using NMOS pull down network. The NMOS device is the positive bias device so the threshold value of the device is frequently changed. A new logic operation has provided (i.e.) feed through logic (FTL) [8], has been introduced, which has proved its high-performance capability. In FTL however, the roles of the clock and logic transistors are interchanged and the clock transistor is In compound domino logic (CDL), dynamic and static gates are alternating between each other, i.e., the output inverter is replaced with a more complex inverting static gate (NAND), such that the monotonicity requirement is satisfied while conducting complex logic operations without wasting the one inverter delay [3]. Except the first stage, all the dynamic stages can be footless in CDL [1]. This logic comes at the cost of increasedpower consumption due to the possible direct now the critical path. Constant delay logic[1] delivered by a local window technique and self-reset technique. CD logic should be used only to replace the critical path in any circuit block, since it doesn't energy efficient to design any system. To identify these problems, the proposed method focuses a new high-performance logic technique. The multi stage circuits are mainly used circuits in the latest circuit design. So the new arrival techniques are create some changes for improve quality of the system.

2. SYSTEM ANALYSIS

In the VLSI system, the commonly used combinational circuit is single bit full adder. The full adder designed by using 28 transistors. The circuit has two blocks, one is sum block and another one is carry block. Figure2. Shows the circuit diagram of the full adder designed with 28 transistors. The circuit is also called as mirror circuit. The PMOS network connection and NMOS connections are same in the circuit.

2.1 Full Adder

The Fig. 1 and 2 shows the block diagram and schematic diagram of the full adder respectively.A one bit full adder is a device with three one bit binary inputs (A, B, Cin) and two one bit binary outputs (Sum, Cout). Taking both carry in and carry out signals, the full adder is highly mountable and found in many cascaded circuit design. The basic logic functions of the full adder can be explained in the truth table. The full adder can also be decomposed into the following logical relationships,

$$S = A \oplus B \oplus C_{IN} \quad (1)$$

$$C = AB + BC_{IN} + C_{IN}A \quad (2)$$

The implementation of the full adder is the Mirror Full Adder. The circuit device uses 28 total transistors (4 transistors used for the design of two inverters). Since the full adder perform a fundamental building-block component to larger circuits , delay and power optimization forces at the adder level. It can lead to improved circuit throughput ratings, speed performance, and lowered power consumption requirements. The fundamental level it is very important to minimize and resolve any timing issues so as to avoid issues predictably brought about by scaling.

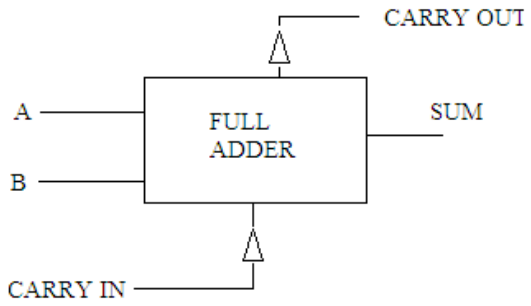

Fig 1. Full Adder

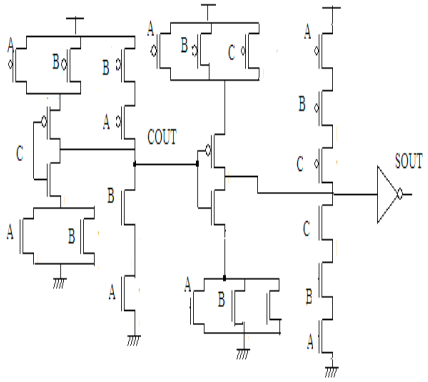

Fig 2. Schematic Diagram

3. EXPERIMENTAL RESULT

3.1 Overview

In the multistage circuit, the output of the previous stage is given to the input of next stage. The sum of the full adder circuit is not given to the next stage input. But the carry output of the circuit is given to the input of next stage. The carry block is designed by using various logic and shown in the figure.

3.2 Static CMOS logic

The carry block designed by using static CMOS logic and also obtained the power and delay value. The equal number of NMOS and PMOS circuit is used for design the carry block. The fig 3. Shows the circuit diagram of the carry block and fig 4. Shows the output wave form of the circuit.

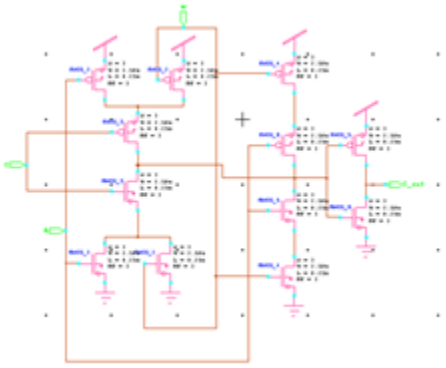

Fig 3. Carry block in static logic

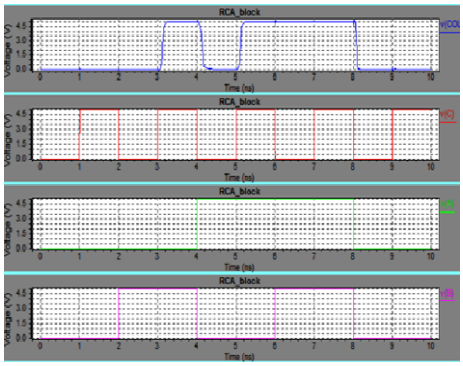

Fig 4. Waveform of carry block

3.3 Dynamic logic

The carry block designed by using dynamic logic and also got the power and delay output. The NMOS network is used for perform the operation. The CLK signal given by using PMOS and NMOS devices. The figure 5. Shows the circuit diagram of the carry block and figure6. Shows the output wave form of the circuit.

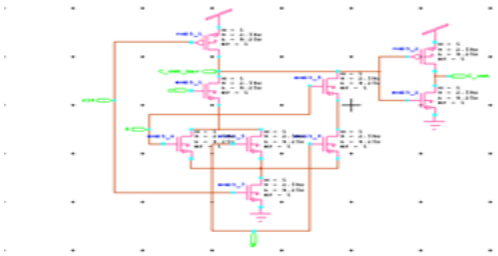

Fig 5. Carry block in dynamic logic

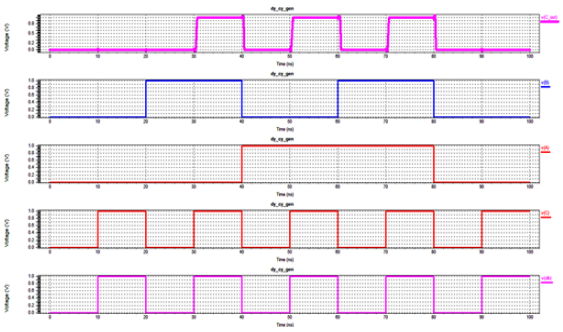

Fig 6. Waveform of carry block

3.4 CD logic

The carry block designed using constant Delay logic and also obtained the power and delay. The operations performed by using NMOS pull up network. The clock signal given by using PMOS device. The additional timing block is used for design the circuit. The figure 7. Shows the circuit diagram of the carry block and figure 8. Shows the output wave form of given circuit.

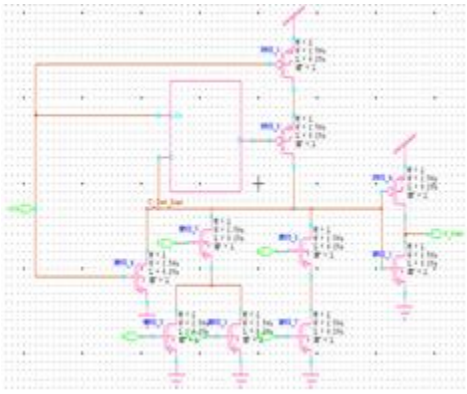

Fig 7. Carry block in CD logic

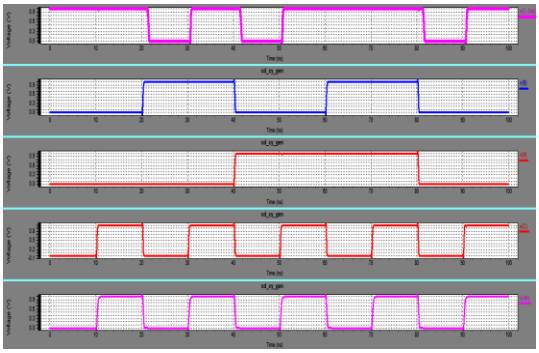

Fig 8. Waveform of carry block

3.5 Proposed logic

The carry block designed by using new logic it derived from CD logic. The PMOS network is used for perform the operation. The clock signal is given to the NMOS network. The PMOS device is the controllable device which has high noise immunity. The power and delay value calculated using simulated tool. The figure 9. Shows the circuit diagram of the carry block and figure 10. Shows the output wave form of the circuit.

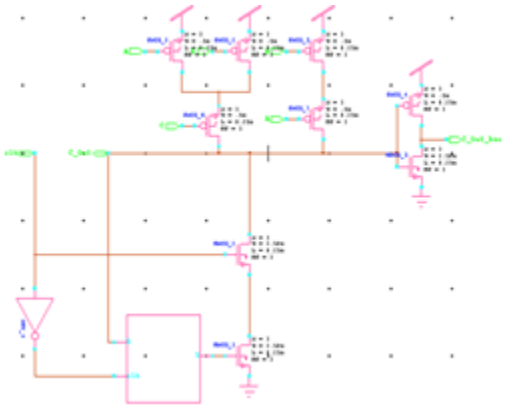

Fig 9. Carry block of proposed logic

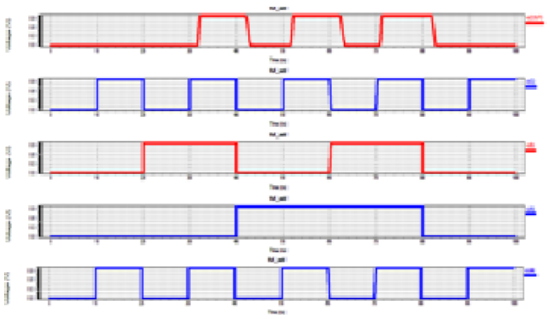

Fig 10. Waveform of carry block

3.6 Comparison Table

LOGIC	FREQUENCY (GHz)	SUPPLY VOLTAGE (V)	POWER CONSUMPTION (µW)	DELAY (ns)
Static logic	0.5	1	17.4	44.3
Dynamic logic	0.5	1	15.0	4.9
CD logic	0.5	1	18.1	20.5
proposed logic	0.5	1	11.6	5.0

4. CONCLUSION

In the multistage adder circuit, the sum output is not given to the next stage. The carry output is given to the input of the next stage. Here, the different logics used for design the carry block. The performance of the circuits is analyzed by using Tanner EDA tool with 1V power supply and 0.5MHz frequency. The future works includes the design of single bit full adder and expand it to multistage adder circuit.

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