Power Reduction In 5T SRAM Cell Using Circuit Level Approach In 45nm Technology

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ABSTRACT: This paper proposes CMOS 5T SRAM cell intended for the power reduction in it for advanced memory design. The aim is to reduce the static power dissipation. Various employed technologies are briefly described and discussed in the best possible way along with their strengths and weakness. The design metrics of a five transistor SRAM cell are discussed briefly and its performance is evaluated. Lastly, comparison between various methodologies is done to evaluate the best methodology to reduce power as per described technology. Performance and delay parameters will also be calculated using the tools, used in the entire project duration (H-spice). It is shown that the power in the new cell will be reduced up to 20% as compared to the conventional cell. As a trade-off, this may affect the area or speed of the cell, up to some extent. The entire work is done using tools like Microwind, DSCH and finally simulation done using H-Spice and thus power reduction. Delay is calculated using Cosmoscope. The technology used is 45nm technology.

Keywords: 5T SRAM cell, CMOS (Complementary Metal Oxide Semiconductor), SRAM (Static Random Access Memory), Static Power Reduction.

1 INTRODUCTION

The need of low power VLSI design is severely increasing now a day. This is because; designers are improving circuit performances and functionalities within the single chip. As a result magnitude of power per unit area is increasing. Shrinking technology also contributes a lot to this issue. Hence, with recent aggressive growth of technology scaling, standby leakage power is increased nearly five times each technology. This thesis presents a low power 5T SRAM cell using Circuit Level Approach. Basically, it is a leakage current reduction technique. By using this, power dissipation is reduced to some extent. This is done using H-spice simulation. Firstly, the circuit design (5T SRAM cell) is done using DSCH tool by generating net list for the same and then the circuit is simulated using H-spice where power reduction is done at the transistor level circuit using appropriate code in H-spice and using appropriate model file in suitable level. Delay is also calculated for each applied technique to maintain reliability of the design. Various other parameters can be seen in the simulation file of H-spice. The advantage of reduced power device is reliability in terms of long life of the system; reduced cooling cost hence reduced cost of the device. This paper is organized with overview of power dissipation in II section. Methodologies adopted are described in section III. Proceeding towards IV section, details of result and comparative analysis is highlighted. V section concludes the final outcome of the research done in the entire workout.

2 OVERVIEW OF POWER DISSIPATION

2.1 Overview

Nano technology results in high chip density and thus more and more switching activity, resulting in power dissipation in any electronic system. Sub micron technology i.e. within the same chip area, engineers are building more and more number of transistors, reducing device dimension. Hence, two things are happening:

(a) Reduced device dimension.
(b) Increase power consumption
(As per Pdc = $VDD^2 * f * C$)

Changing trend of devices from BJT → MOSFET → CMOS → Bi CMOS etc. i.e; from SSI → MSI → LSI → VLSI → ULSI → GSI, for better circuit performance, area, delay, power etc. But due to this switching activity is increased and thus charging and discharging of transistors results in power dissipation. If the device is compact, process parameters will obviously increase (like aspect ratio, threshold voltage etc.). This process parameters are variably due to scaling (variation in parameters of device with respect to device trend is called as Scaling). Today we prefer CMOS technology due to convenience in:

(a) Easy fabrication
(b) Good noise margin as compared to BJT, TTL, ECL etc.
(c) Low switching activities
(d) No charge sharing problem
(e) Static power dissipation we can manage to almost zero here.

But still there are few disadvantages as:
(a) Glitch power dissipation
(b) Short circuit power dissipation
(c) Large number of standard cells to manage.

2.2 Sources of Power Dissipation

Sources of Power Dissipation in CMOS technology which chip dissipates per unit area:

(a) Static Power Dissipation
(b) Dynamic Power Dissipation

Mathematically,
Total Power= Static Power Dissipation + Dynamic Power Dissipation

We will focus here on Static Power Dissipation or Inactive Power Dissipation here which occurs due to:
(a) Gate leakage current
(b) High parasitic capacitance
(c) Switching action of transistors
(d) Diode leakage current
(e) Sub threshold leakage current etc.

There are lots of techniques which reduce power dissipation and make low power SRAM cell reliable from the power point of view. Here we will focus upon static power dissipation. Technology is shrinking rapidly these days which is leading to high parasitic capacitance which ultimately resulting in leakage power. This exists when the circuit is inactive i.e. no input is given for the circuit to response for output. Since, no input is given the supply is cut. But still, circuit is not completely off and some leakage power is continuously flowing in the circuit. This we define as leakage power. Whereas, dynamic power is consumed when the circuit is active, i.e. when input is given to circuit and is enabled with the main supply. Because of the shrinking technology problem of static power dissipation arises by continuous switching action. Given below is the description of the causes of static power dissipation:

(a) Leakage due to Sub threshold current: The current less than IGS threshold current, called as sub threshold current which drops rapidly causes leakage current.

(b) Gate Tunneling Leakage Current: Due to transistor scaling, the gate oxide thickness is also reduced to great extent which allows small amount of current not to pass through it which leads the transistor to be ON to very small extent and thus results in leakage current. Hence, there is leakage power dissipation due to the presence of sub threshold and gate tunneling leakage currents. Short circuit and switching are basically, the types of dynamic power dissipation whereas sub-threshold leakage current and gate tunneling leakage causes static power consumption. Parasitic capacitances are charged and discharged during the logic transition in dynamic power dissipation. But, static power dissipation is one in which leakage current is flowing through the transistors even when the inputs and outputs are not changing.

3 METHODOLOGY

3.1 5T SRAM Cell Functionality

(a) Write Operation: In order to perform write operation firstly we need to enable SRAM cell
by mean of enabling the access transistor by giving logic “1” to the gate terminal of it. Once the cell is enabled, through write driver transistor from source or drain terminal supply logic “0’” or “1” enabling the transistor. The data will travel from the transistor to the bit line and will be stored in the cell. In Q terminal original written value will be stored and in Qb its complement.

(b) Read Operation: To read the data already stored in the cell we will use read buffer that is chain of inverters. This chains of inverters will be connected to the source/ drain terminal of the enabling transistor and one with bit line. Its gate terminal will be supplied with logic “1” to enable the transistor. As soon as the buffer will be enabled, the data stored in the cell will be read from the buffer output.

(c) Standby Mode: When WL= 0, then the cell will be off and hence the data which is stored in the cell will remain as it is. Until and unless the SRAM cell will be enabled the circuitry will remain in standby mode. Design Schematic of 5T SRAM cell along with operations in a sequence of writing “0” and then reading “0”, then writing “1” and reading “1” is done using Design Schematic tool and circuit simulation in H-spice. Avanwaves respectively for the same is given below:

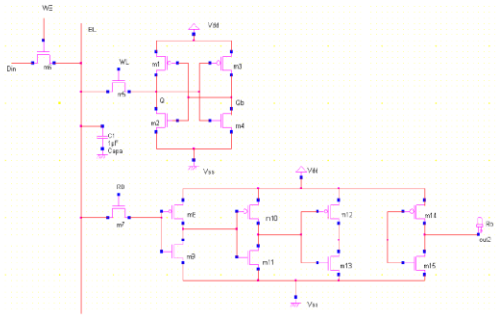

Fig.1 *5T SRAM cell Design Schematic*

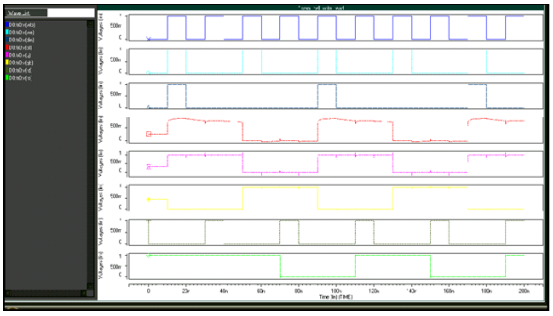

Fig.2 *Read and Write Operation in 5T SRAM Cell*

3.2 Implementation of Techniques in 5T SRAM

(a) Sleepy NP Transistor Technique
Here additional sleepy PMOS and sleepy NMOS transistor is added in VDD and GND respectively in an SRAM cell. This will cut off the power rail throughout the cell in sleep or standby mode thus restricting the leakage power in the circuit. Power reduced by this technique is 14.08%. Delay for write ‘0’ is calculated to be 8.009p and read ‘0’ is 61.94p. For write ‘1’ is 27.3p and read ‘1’ is 32.64p. Represented below is the design schematic in fig.3 and simulation waveform in fig.4.

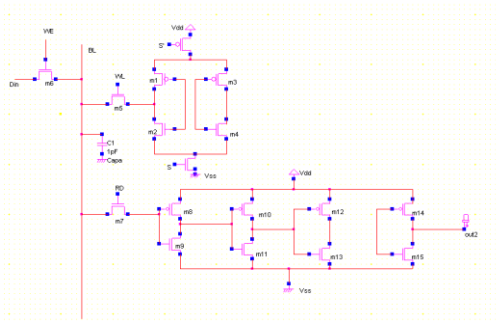

Fig.3. *DSCH of 5T SRAM cell with Sleepy NP technique*

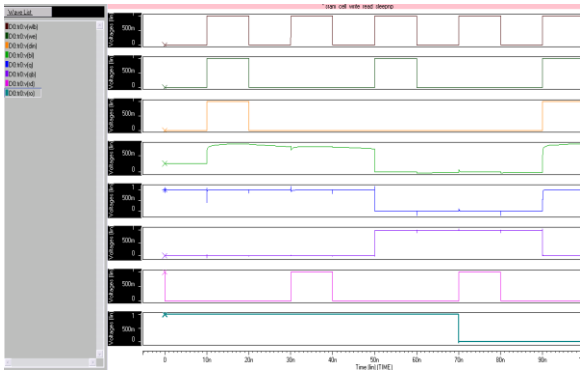

Fig.4. *Simulation waveform for Sleepy NP 5T SRAM Cell*

(b) Sleepy Keeper Technique

Sleepy keeper utilizes leakage feedback technique. In this technique, NMOS transistor is placed in parallel to the sleep 'P' transistor and a PMOS transistor is placed in parallel to the sleep transistor 'N'. These two additional transistors will be conducting by the output of 5T SRAM cell. During standby mode or off mode, sleep transistors will be turned off and another transistor in the parallel to the sleep transistor will keep the connection with the suitable power rail. The representation is given in Fig.5 and waveform in Fig.6. The reduced power found in this technique is 14.03%. Delay for write '0' is found to be 7.86p and read '0' is 61.36p and write '1' is 27.45p and read '1' is 34.80ps.

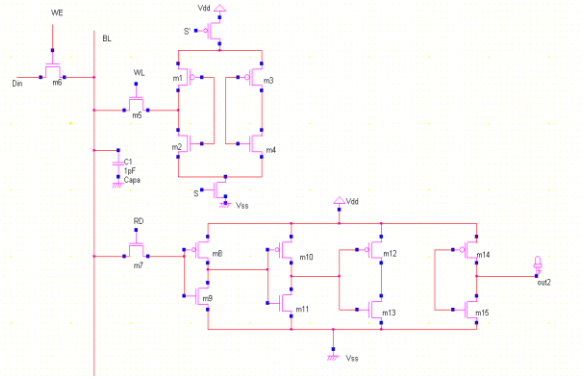

Fig.5. *Sleepy Keeper 5T SRAM cell*

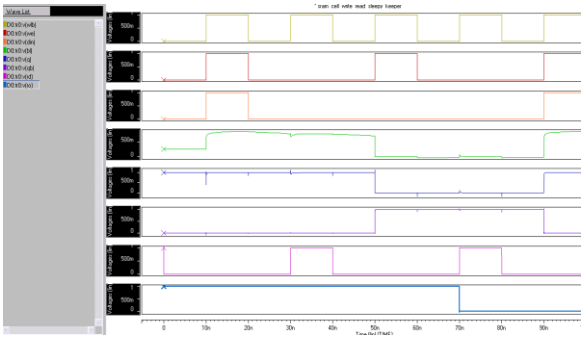

Fig.6. *Simulation waveform for Sleepy Keeper 5T SRAM Cell*

(c) Dual Sleep Technique

As the name suggests, dual sleep technique is a method utilizing two extra pull-up and pull- down transistors. These should be in sleep mode, either in ON or OFF state. This portion of extra pull up and extra pull down transistors is made common to the whole circuitry; less number of transistors is utilized to apply some logic circuitry. Illustration of design schematic and simulation waveforms is given in fig.7 and fig. 8. Reduced power is up to 18.63%. And write '0' delay is calculated to be 7.91p, read '0' delay is 61.23p. Write '1' delay is 27.47p and 84.79p is read '1' delay.

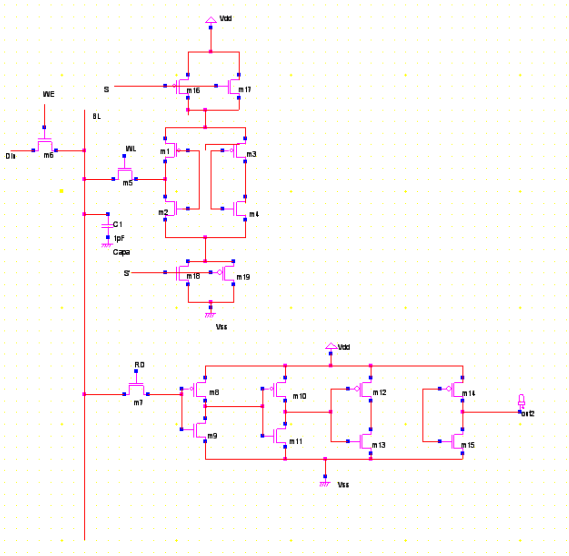

Fig.7. *Dual Sleep Technique 5T SRAM cell*

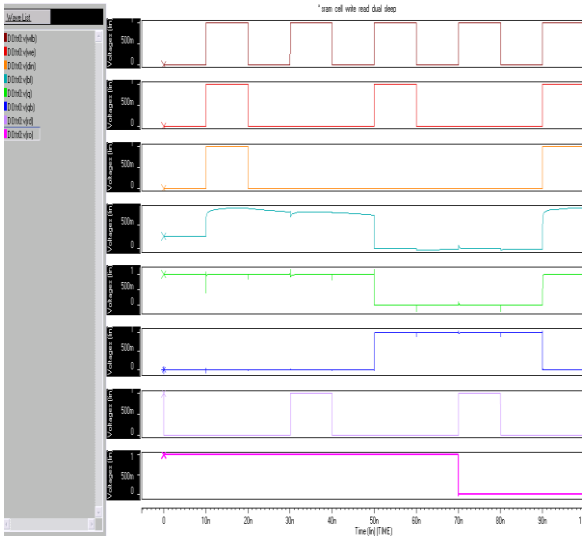

Fig.8. *Simulation waveform for Dual Sleep 5T SRAM Cell*

(d) Dual Stack Technique

In dual stack technique, along with the sleep PMOS and NMOS transistor, two NMOS in series and two PMOS in series respectively are placed. By this arrangement of transistors, NMOS will be inactive at logic '1' and PMOS at logic '0'. Power supply will be cut down and thus leakage power will be diminished. The circuitry is given in fig.9. Power reduced in this technique is 19.02%. Write '0' delay is calculated to be 7.91p, read '0' delay is 61.23p. For write '1' de-

lay is 27.45p and read '1' is 84.79p. Design schematic and simulation waveforms are illustrated in fig.9.and fig.10.

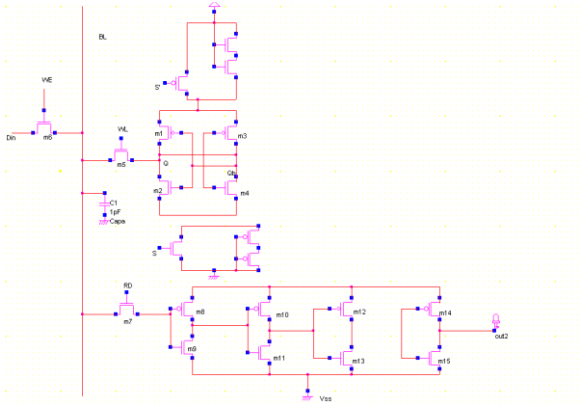

Fig.9. *Dual Stack Technique 5T SRAM Cell*

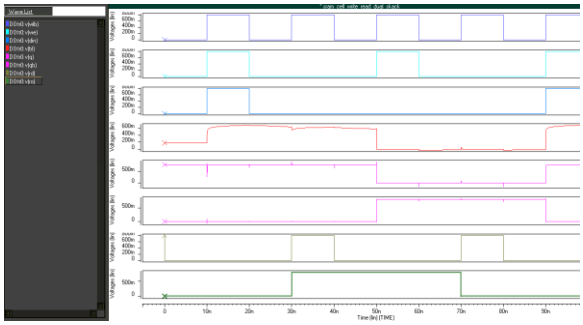

Fig.10. *Simulation waveform for Dual Stack 5T SRAM Cell*

4 Result And Comparative Analysis

4.1 Result

The final result drawn out of the entire research work with description of power dissipation in standard SRAM cell and reduction in it after adopting various techniques is given below. Delay is also shown unaffected and lastly comparative analysis of different methods done is given.

Table.1. *Power dissipation and Reduction percentage in 5T SRAM cell using H-spice*

Technology (nm)	Techniques	Power (mw)	Reduction (%)
45nm	Conventional	0.018	-
45nm	Sleepy NP	0.015	16.66
45nm	SleepyKeeper	0.015	16.66
45nm	Dual Sleep	0.014	22.22
45nm	Dual Stack	0.014	22.22

Hence it is found that all these four techniques work better for leakage power reduction as Sleepy NP and Sleepy Keeper technique contributes to reduce 16% power, but Dual Sleep and Dual Stack Technique is found to be more better as it contributes approximately 22% of the leakage power reduction. Further after calculating the average power consumption in all the methodologies in 5T SRAM cell, delay is calculated. It is found that delay is not disturbed at all during entire workout i.e. delay is same for all techniques approximately with slight decrement in it but not increment. The table is given below in table 3.5.2 (b), illustrating the delay parameters for read and writes both operation for both "0" and "1" logic.

Table.2. *Read and Write delay in 5T SRAM cell*

Techniques	Write Delay (ps)		Read Delay (ps)	
	Write "0"	Write "1"	Read "0"	Read "1"
Conventional	7.9	29	61.4	35.4
Sleepy NP	8	27.3	61.9	35.4
Sleepy Keeper	7.8	27.4	61.3	34.8
Dual Sleep	7.9	27.4	61.2	34.8
Dual Stack	7.9	27.4	61.2	34.8

4.2 Comparison from previous work

Given below is the table which shows comparison between some other methods and this method of power reduction. After proper study and comparison it is found that Dual Stack/ Dual Sleep reduces more power than these two methods without affecting delay for both read and write operation.

Table.2. *Comparative Analysis of the different low power techniques*

Technique	Average Power (mw)	Reduction (%)
Dual Stack and Dual Sleep	**0.014**	**22.22**
Conventional Analysis	38.05	-

5 Conclusion

It is found out from the entire work out that adopting all the four techniques, Dual Stack and Dual Sleep works best with decrement of 22.22% of total power calculated with not affecting delay. Further by comparative analysis these two techniques were found out to be reliable as it reduces more amount of power. Difference between Dual Stack and Dual Threshold is calculated to be 93%. That is Dual Stack is 93% better than Dual Threshold and 88% better than low power design in 180nm technology with an advantage of reduced technology i.e. 45nm.

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