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Waveform Generation Using Xilinx System Generator

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ABSTRACT: Efficient and effective control of electrical equipments needs digital signal processing unit. The power electronics devices control the motor and electrical equipments and the devices are switched by controllers. The reference signals are generated for the controller for effective switching of Power devices. Various signals are generated in MATLAB Simulink platform which is required for control applications and for real time implementation Xilinx system generator is used.

Keywords : Power electronics; controller; MATLAB; Simulink; Xilinx; System generator

1 INTRODUCTION

Many processors are used to generate waveforms for various control algorithms. Microprocessor, Microcontroller, DSP and FPGA are the Processor generates waveform for variety of applications. Main criteria of the processor are the speed, memory space and heat consumption[1-3]. FPGA is the one which satisfy above criteria and the signal generated by writing VHDL / Verilog coding or building block using Xilinx system generator. Spartan 3A DSP Trainer kit has the FPGA processor, 8 Nos of digital input using dip switches, 16 Nos of digital outputs using discrete LEDs, One Reset switch, FPGA configuration through JTAG port and Onboard Flash Prom XCF16PV048, On board programmable oscillator from 3MHz to 100 MHZ, 16 × 2 LCD interface, ADC & DAC interface, Add on card VSDA - 03 for ADC & DAC with SDA bus, RS232 Serial Port designed by Vi Micro System PVT[4-5]. Power electronics devices are controlled by the above processor because of its simple configuration , IO lines and more number of PWM pins.

2 SPARTAN 3A DSP

Figure 1. shows the Spartan 3A DSP Trainer kit interfaced to the MATLAB by JTAG connector and ADC to ADD on card. Capture and IO pins are available and also 50 number of PWM pulses are generated by the processor which is in very high value compare to DSP(Digital signal processor)[4].

1. Spartan 3A DSP
2. PLL clock settings
3. JTAG connector
4. RS 232 serial port
5. Parallel port
6. LCD display
7. PWM connector
8. SDA Bus connector
9. Power supply
10. USB

3 WAVEFORM GENERATION

The 1Φand 3Φ sine waveform is generated by the Xilinx tool box of MATLAB Simulink. The specifications of system generator and waveform generator tool is given in Table –I - Table – VI. The signal are generated for 50 Hz frequency

4 FPGA PROCESSOR WITH MATLAB

The bit file generation, interfacing with board and Xilinx diagram of the waveform generation is shown in fig 2, fig 3 and fig 4. The specifications for the tool box are given in the above table. The input is the zero crossing detector of any reference signal to obtain the origin for the generation of waveform. Once the model is created, bit file is generated by system generator blockset and it is stored in netlist. Connect the PC to the FPGA processor through JTAG. Open Xilinx ISE Design Suite 12.2 – ISE Design Tools – Tools –iMPACT. Open Boundary Scan, right click – Initialize chain . right click Xilinx 1800a – Assign New Configuration – netlist folder – select bit file. Right click Xilinx – program. The program dumped in the Processor and waveforms are observed in Digital storage oscilloscope without using DAC.

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Table – I

System Generator specifications

System generator	Specifications
Compilation	Bitstream
Part	Spartan -3A DSP xc3sd1800a-4fg676
Target directory	./netlist
Synthesis tool	XST
Hardware description language	VHDL
FPGA clock period(ns)	50
Clock pin location	F13
Multirate implementation	Clock Enables
DCM input clock period(ns)	10
Simulink system period	1

Table – II

IOB pad locations

Gateway	IOB pad locations
Out2	G9
Out3	D10
Out4	G6
Out6	W3
Out8	V1
Out10	U1
In	AC3

Table – III 3Φ sine wave generation

TERMS	ROM 1	ROM 2	ROM 3
Basic – Depth	200	200	200
Initial value vector	256(sin(2*pi*(0:199)/199))	256(sin((2*pi*(0:199)/199)+133))	256(sin((2*pi*(0:199)/199)+67))
Memory type	Block RAM	Block RAM	Block RAM
Word type	signed	signed	signed
Number of bits	9	9	9
Binary point	0	0	0
Latency	1	1	1

Table –IV 3Φ cosine wave generation

TERMS	ROM 1	ROM 2	ROM 3
Basic – Depth	200	200	200
Initial value vector	256(cos(2*pi*(0:199)/199))	256(cos((2*pi*(0:199)/199)+133))	256(cos((2*pi*(0:199)/199)+67))
Memory type	Block RAM	Block RAM	Block RAM
Word type	signed	signed	signed
Number of bits	9	9	9
Binary point	0	0	0
Latency	1	1	1

Table – V Triangular wave Generation

Terms	Counter
Counter type	Count limited
Count to value	199
Count direction	Up
Initial value	-1
Step	1
Output type	Signed
Number of bits	8
Binary point	0
Optional ports	-
Explicit period	2000

Table –VI Counter specifications

Terms	Counter	Counter 1	Counter 2
Counter type	Count limited	Count limited	Count limited
Count to value	99	199	1000
Count direction	Up	Up	Up
Initial value	0	0	-1000
Step	1	1	1
Output type	Unsigned	Unsigned	Signed
Number of bits	8	8	13
Binary point	0	0	0
Optional ports	Provide enable port	Provide synchronous reset port	-
Explicit period	2000	2000	1

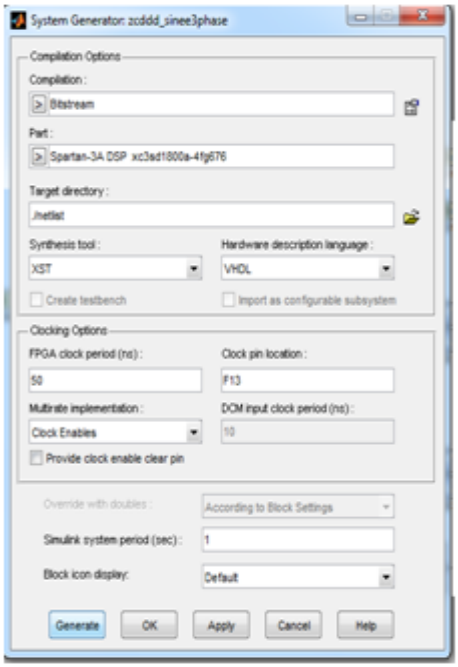

***Fig 2**. bit file generation*

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Fig 3. *Interfacing with FPGA board*

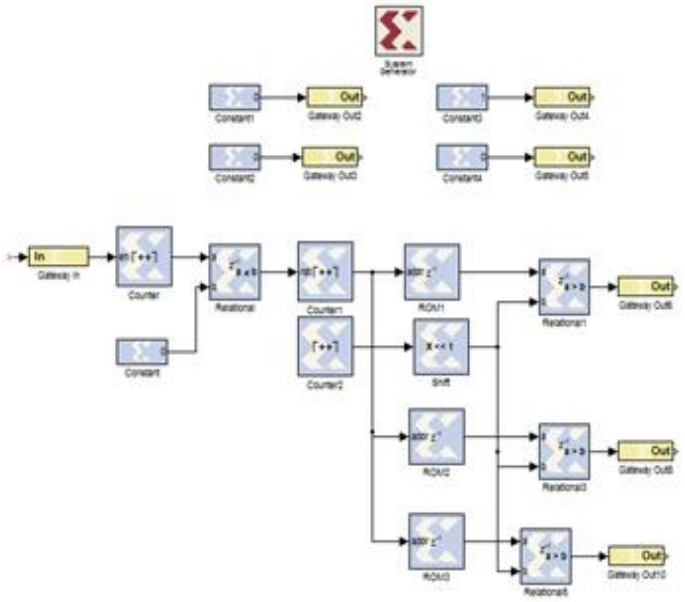

Fig .4*. 3Φ sine wave generation*

5 CONCLUSION

The 3Φ sine wave, cosine wave and triangular wave is generated using MATLAB Simulink Xilinx tool box. Simulink is user friendly tool box and model is created easily and interfaced to FPGA processor without the knowledge of VHDL / Verilog coding. JTAG interface the Xilinx with the processor. The waveforms are observed without DAC unit

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