A Low Power And Reliable 12T SRAM Cell Considering Process Variation In 16nm CMOS

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ABSTRACT: In this paper a new 12T-SRAM cell employing 16nm CMOS technology is introduced. The cell has separate read and write paths. For reducing the power consumption, this cell inserts a transistor for isolating the supply voltage rail from cell. This transistor acts as a power gating transistor in hold mode and feedback in active mode. Also this transistor with weakening the cell in active mode, improves the write access time and write margin. The read path of proposed cell buffers by two transistors which reduces its leakage current corresponds to the stacking effect. This cell deforms the butterfly diagram and increases the available SNM. In comparison of proposed cell with 9T SRAM and Schmitt trigger 10T (SC10T) structures shows that proposed cell has 75.5% and 4.6% higher read SNM and 25% and 20% lower write access time respect to 9TCell and ST10T cells respectively. The hold power of proposed cell is also 4.24X and 4.17X lower than the other cells.

Keywords: SRAM Cell, SNM, Reliability, Process variation

1 INTRODUCTION

Over the last few decades, scaling of conventional CMOS technology has been created two main problems; reliability and power consumption[1, 2]. The supply and threshold voltage are scaled with scaling process. So, the static power increases significantly corresponds to exponential dependency of leakage power to threshold voltage. Moreover, changing the characteristic of the each transistor due to process variation. These problems become critical in the case of SRAM memories which are occupied most parts of nowadays chips. The memories are the main source part of power consumption so reducing the supply voltage for working in sub and near threshold is important. Designing the SRAMs with lower power and higher stability are the challenges of this field. Reducing power consumption of memories is extremely important since the maximum area and power of a sample IC is dedicated to memories such as SRAM which are usually operate with static power consumption. Reducing the supply voltage in this area improves the total energy consumption of the processor hugely. There are a lot of ways for reducing the power consumption of the digital designs such as reducing the supply voltage, using staking effect[3], power and clock gating technique[4, 5], multi threshold voltage and Dynamic voltage Scaling[6]. Reducing the supply voltage to near and sub threshold is one of the method of power reduction of digital circuits. So the new researches focus on designing the subthreshold SRAM cell with higher reliability in these voltages [7-9]. Consideration process variation effect in power and delay of new devices increases the challenge of low power SRAM design[10]. This paper is introduced low power SRAM cell which is power gated in hold mode and has an ultra-low power leakage in its read paths.

2 PROPOSED SRAM CELL STRUCTURE

2.1 Cell's Operational Modes

The proposed SRAM cell is demonstrated in Fig 1.This structure consist of ten transistors which six main transistors are same as conventional 6T. The four additional transistors respect with 6T are used to separating the read and write path of cell. The cell is single ended structure which does the read operation from one side of cell. Using separated path for read and write operation increases the control over the array of the cell in the catch design by simultaneous read and write operations which is in contrast with shared access path as conventional 6T cell. Circuit functionality modes are; Write, read and hold mode. The state of the control signals for choosing between these modes is archived in Table 1. The WWL and RWL are independent signals and Hold Signal (HS) is produced by them (see Fig 1). Both write and read modes are called active mode. For choosing between active and idle (hold) mode, M12 transistor is used on the top place which separates virtual supply voltage from supply voltage rail. This transistor acts as a power gating transistor. In active mode the M12 transistor should be in ON mode by producing zero in HS signal (HS=0). After that the write and read operation can be done. The characteristic of cell in different modes is discussed in below parts.

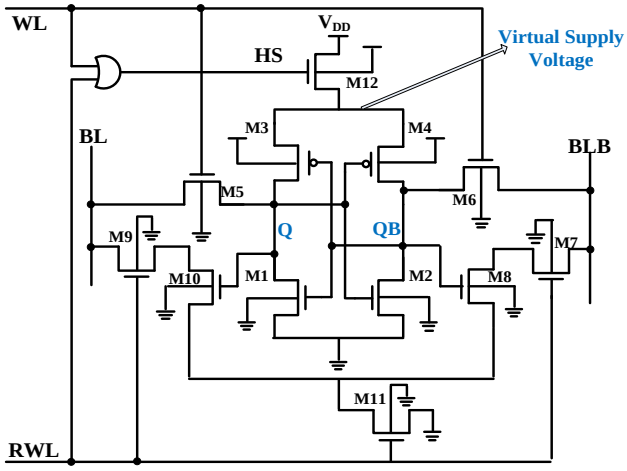

Fig 1. Proposed 12T-SRAM cell structure.

Table 1. The control signals in different operation modes

Cell modes	WWL	RWL	HS=(WWL) OR (RWL)
Read	0	1	1
Write	1	0	1
Hold	0	0	0

Write Operation

The write paths proposed architecture consist of two transistors (M5 and M6). In write mode, these transistors activate with WWL signal and write the value of BL and BLB

on the storage nodes. The write operation can be performed at supply voltages as lower voltage. Inability of access transistors to change the cell's value in write operation is called write failure.

2.2 Read Operation

The read operation is done only from QB storage node. In this mode RWL signal becomes one and Bl and BBL pre-charge to one. When cell saves the one, (Q=1 and QB=0) the M10 becomes ON and reads the Q node by passing the current through M8 and M9. On the other case, when zero is saved in cell (Q=0 and QB=1) the M8 becomes ON and BLB line discharges thorough M7 and M11.

3 RESULTS AND DISCUSSION

The proposed SRAM cell architecture is compared to 9T[11] and Schmitt trigger 10T[12] cell based on characteristics such as: write access time, write margin, power dissipation and SNM. All structures are designed by using low power 16nm Predictive Technology Model (PTM). The 9T and SC10T structures are shown in Fig 2 and Fig 3 respectively. In proposed architecture the read and write paths are formed by two different access transistors which result in higher Static Noise Margin (SNM) of the cell. This architecture uses from two stage buffer for isolating the read path from bit line. In addition M12 transistor, using M7, M9 and M11 causes isolating the read paths and reducing the leakage. So, this structure has very low standby leakage. Also the write access time of proposed architecture is improved because of charging the virtual supply voltage node which can weaken the loop. It results that the bit lines have more control in inverters loop. In this structure the data is ready for access transistors in read phase. The data is ready in the storage loop and M7 and M8 transistors are activated by the side of the loop which is holding "1". This can accelerate the charging of bit line through the access transistors by arrival of word line signal. As a result, decreasing the write delay, increasing the SNM and also some improvement in hold power consumption of proposed architecture makes it reasonable.

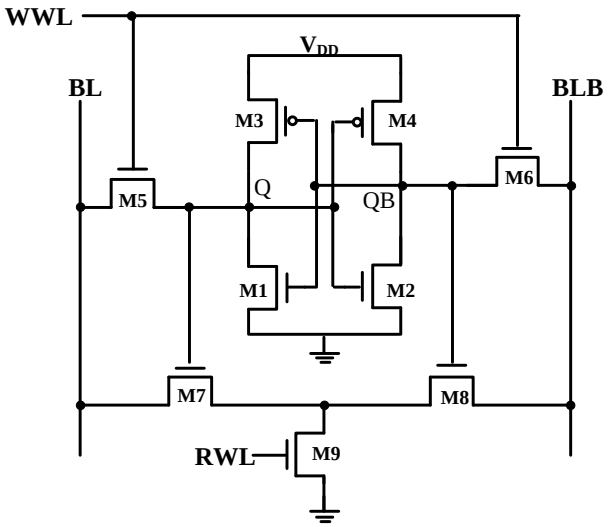

Fig 2. 9T SRAM cell[11]

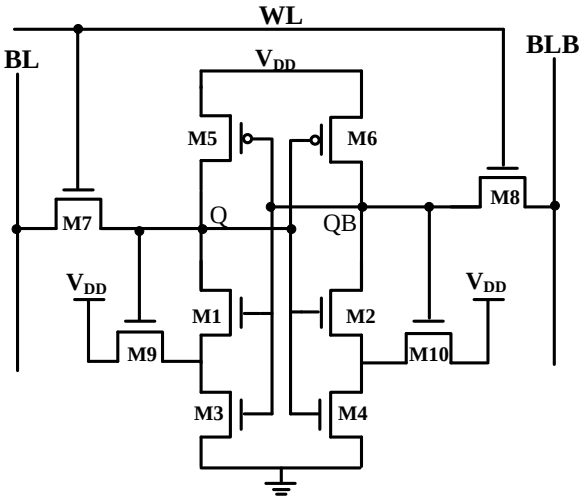

Fig 3. Schmitt trigger SRAM cell [12]

This paper uses the low power library of 16nm technology [13]which has high threshold voltage near the 600mV. The results are determined 800mV supply voltage. The butterfly diagrams of read operation for different cells in 800mV supply voltage are compared in

Fig **4**. The accurate SNM value of the structures is written in figures legend. The comparison indicates that proposed cell has 5.5% and 27.4% higher read SNM from 9T and ST10T cells respectively. The hold SNM of the proposed architecture computes when 400mV is applied to HS in above threshold for gating to sleep mode. As the figure shows, gating the cell reduces the hold SNM of cell but due to high stability of cell, this reduction does not hugely matter in hold mode. The comparison of structure shows that proposed structure with HS=0 has high reliability. By applying the 400mV to HS, the hold power becomes 20mV lower. This voltage can significantly reduce the hold power of cell due to reducing the dropped voltage across the cell.

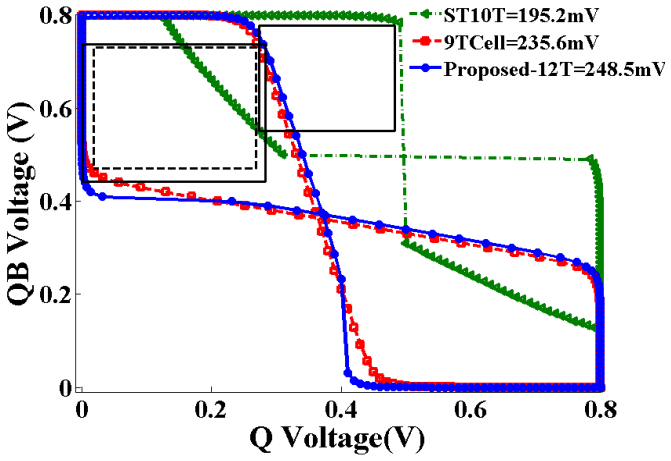

Fig 4. Butterfly diagram for read operation in 0.8V supply voltage

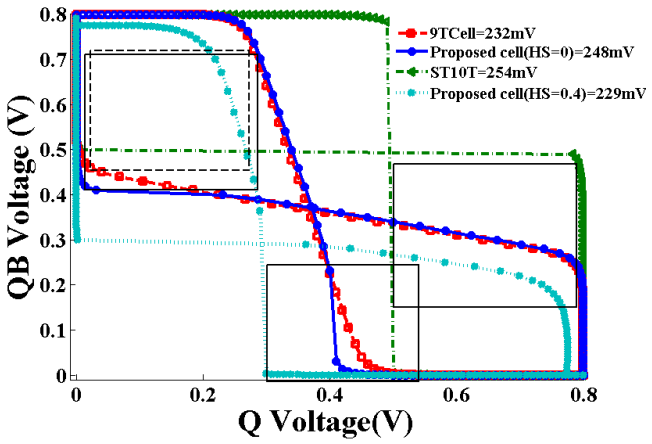

Fig 5. Butterfly diagram for Hold operation in 0.8V supply voltage

The characteristic parameters of proposed cell such as Read and hold SNM, write access time, write margin and hold power in comparison of 9TCell, ST10T structures are archived in Table 2. The power comparison of proposed cell with other structures demonstrates that proposed cell has 35.5% and 43.6% lower hold power in comparison of 9Tcell and ST10T respectively.

Table 2. Characteristics of structures in above threshold voltage (Vdd=800mV) and HS=400mV in hold mode

Structures	SNM (mV)		Write		Power
	Read	Hold	Access Time(Ps)	Margin (mV)	Hold (PW)
9T	235.6	235	56.69	356	85.9
ST10T	195.2	254	54.73	226	98.2
Proposed cell	248.5	229	53.62	430	55.3

The read SNM variation in respect with supply voltage is plotted in Fig 6. This shows the SRAM cell's stability is hugely related to supply voltage. As figure elucidates the proposed Structure has more stability in read mode respect with all other structures. Indeed, new SRAM structures with the same main body have similar SNM. The reduction of SNM occurs due to read path leakage current which inject from main body. This current is eliminated in new SRAMs by connecting the gate of read path transistor to the storage node. The little difference between structures comes from the buffering of read path which reduces the leakage by stacking effect. The read SNM variation in respect with supply voltage is plotted in Fig 6. This shows the SRAM cell's stability is hugely related to supply voltage. As figure clarifies the proposed structure has more stability in read mode respect with other structures. The proposed cell with change in main body and exerting an extra transistor can create distortion on the butterfly diagram and make it more square shape. This increased SNM is very important specific in lower supply voltage such as near threshold voltage region.

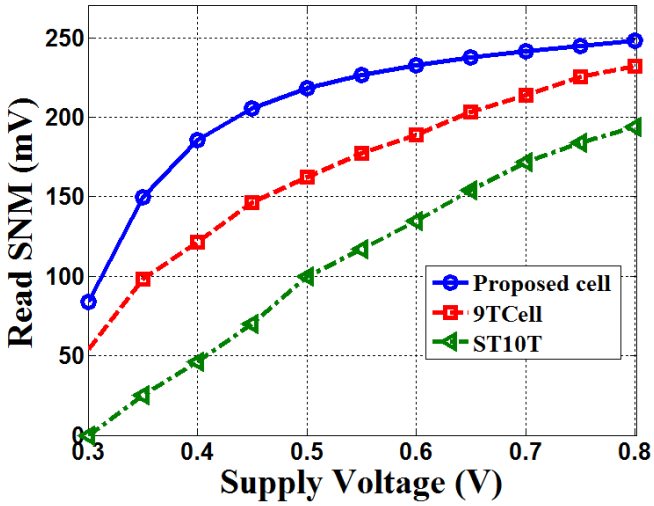

Fig 6. Variation of the read SNM versus supply voltage

The write operation has been done by activation of the word line and writing the BL and BLB data in the back to back inverter. In this state, the read path is completely disconnected and doesn't have significant effect on the write access time. The M12 transistor weakens the invertor loop in active mode and causes the data easily written in cell. The write characteristics of the cell compare to other structures is demonstrated in Fig 7.

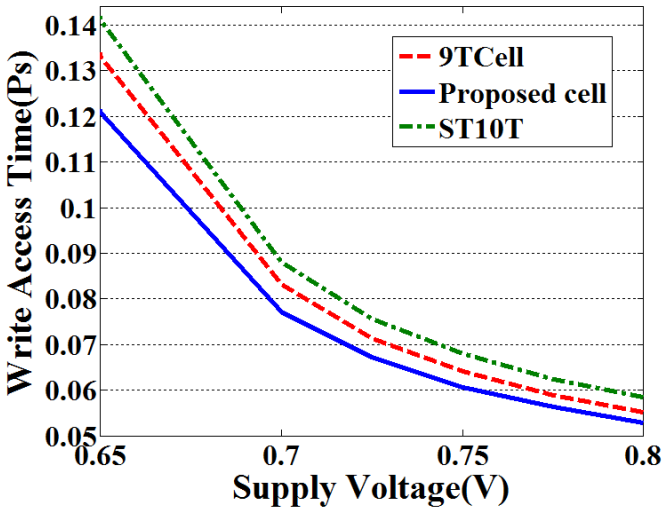

Fig 7. Write access time versus supply voltage

Process variation can change the characteristic of transistor and cause failure in system. This variation is considered in digital circuit as a parameter for figure out the reliability of circuit. The read and hold butterfly diagrams with considering the variations versus 10% variation in size and threshold voltage of transistors are demonstrated in Fig 8 and Fig 9 respectively. It is result of 1000 Monte Carlo simulation with HSPICE 2011. The distributions are shown in figures.

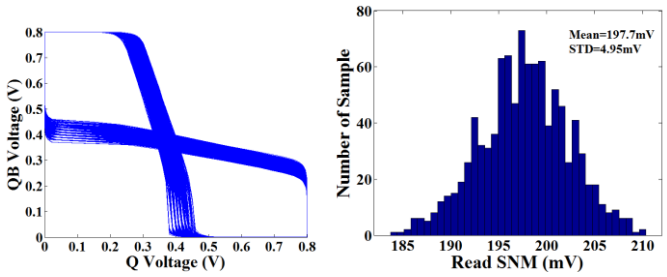

Fig 8. The read butterfly diagram and SNM distributions at supply voltages voltage 800 mV with HS=0

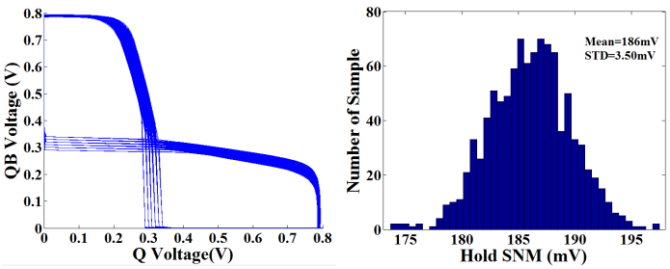

Fig 9. The hold butterfly diagrams and SNM distributions of proposed cell at supply voltages voltage 800 mV with HS=400mV

4 CONCLUSION

This paper introduced a 12T SRAM cell which is efficiently works in 800mV supply voltage employing 16nm bulk CMOS technology. The cell is stacked with a transistor to reduce the hold power. Two stack transistors are used in the read path to reduce the cell leakage and increase stability of the cell. With interning the circuit to the sleep of hold mode the power of cell hugely reduces corresponds to the power gate transistor. Also the cell improves its reliability by increasing the read SNM. The characteristics of proposed cell in comparison to 9TCell and ST10Tcell are discussed in the paper.

REFERENCES

[1] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low-power CMOS digital design," *IEICE Transactions on Electronics,* vol. 75, pp. 371-382, 1992.

[2] M. Jafari, M. Imani, and M. Fathipour, "A 13 ENOB and 40MS/s Switched-Capacitor Sample & Hold Circuit Using a Two-Stage OTA with non-ideal components available in CMOS 0.18 µ technology."

[3] M. Muker and M. Shams, "Designing digital subthreshold CMOS circuits using parallel transistor stacks," *Electronics letters,* vol. 47, pp. 372-374, 2011.

[4] H. M. Vo, C.-M. Jung, E.-S. Lee, and K.-S. Min, "Dual-switch power gating revisited for small sleep energy loss and fast wake-up time in sub-45-nm nodes," *IEICE Electronics Express,* vol. 8, pp. 232-238, 2011.

[5] H. Mahmoodi, V. Tirumalashetty, M. Cooke, and K. Roy, "Ultra low-power clocking scheme using energy recovery and clock gating," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on,* vol. 17, pp. 33-44, 2009.

[6] S. Dighe, S. Vangal, P. Aseron, S. Kumar, T. Jacob, K. Bowman*, et al.*, "Within-die variation-aware dynamic-voltage-frequency scaling core mapping and thread hopping for an 80-core processor," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, 2010, pp. 174-175.

[7] W.-B. Yang, C.-H. Wang, I. Chuo, and H.-H. Hsu, "A 300 mV 10 MHz 4 kb 10T subthreshold SRAM for ultralow-power application," in *Intelligent Signal Processing and Communications Systems (ISPACS), 2012 International Symposium on*, 2012, pp. 604-608.

[8] A. Islam and M. Hasan, "Variability aware low leakage reliable SRAM cell design technique," *Microelectronics reliability,* vol. 52, pp. 1247-1252, 2012.

[9] G. Chen, D. Sylvester, D. Blaauw, and T. Mudge, "Yield-driven near-threshold SRAM design," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on,* vol. 18, pp. 1590-1598, 2010.

[10] M. Ansari, M. Imani, H. Aghababa, and B. Forouzandeh, "Estimation of joint probability density function of delay and leakage power with variable skewness," in *Electronics, Computer and Computation (ICECCO), 2013 International Conference on*, 2013, pp. 251-254.

[11] Z. Liu and V. Kursun, "Characterization of a novel nine-transistor SRAM cell," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on,* vol. 16, pp. 488-492, 2008.

[12] J. P. Kulkarni, K. Kim, and K. Roy, "A 160 mV robust schmitt trigger based subthreshold SRAM," *Solid-State Circuits, IEEE Journal of,* vol. 42, pp. 2303-2313, 2007.

[13] A. Agarwal, H. Li, and K. Roy, "DRG-cache: a data retention gated-ground cache for low power," in *Design Automation Conference, 2002. Proceedings. 39th*, 2002, pp. 473-478.