Enhancement Of H-Bridge Multilevel Inverter Designed With The Avoidance Of Capacitor Voltage Balancing Problem Using Fpga

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ABSTRACT: A single phase multilevel inverter for dcto ac conversion is developed with minimum number of power electronic devices and isolated DC sources with implementation using FPGA. The total harmonics of the output waveform is reduced by increasing the switching modes with reduced devices. The H-Bridge multilevel inverter has two inverters connected in cascade. The proposed inverter can output more numbers of voltage levels in the same number of switching devices by using this conversion. The number of gate driving circuits is reduced, which leads to the reduction of the size and power consumption in the driving circuits. The total harmonic of the output waveform is also reduced. The proposed inverter is driven by the hybrid modulation method.The hybrid modulation algorithm is simulated using MATLAB/Simulink. The VHDL code for each of this topology was written and synthesized using Xilinx ISE software. Behavioral Simulation was performed on the architecture and after verifying the results this VHDL code was downloaded to SPARTAN 3A DSP board.

Keywords: Field Programmable Gate, Array(FPGA),Direct Current(DC),Very High Speed Description Language(VHDL).

I. INTRODUCTION

In recent years, vehicle manufacturers have been faced with the problem of developing a solution to the growing energy crisis and environmental issues. Therefore, electric vehicles (EVs), hybrid EVs, and fuel cell vehicles are studied all over the world [1]–[6]. One of the issues raised in these studies is the limitation of switching devices[1]. If the devices which can sustain high voltage are used in the inverter, their switching frequency is restricted. On the other hand, when the rotation speed of the motor becomes high, the frequency of the reference waveforms also becomes high. When the frequency of the reference waveforms becomes close to the restricted switching frequency, the output waveform is distorted, and the reliability of the motor is reduced. As a provision against the problem, the device voltage must be reduced to use high-speed switching devices. In dc–dc converters, there is a method for reducing the device voltage which divides the voltage by the capacitors connected in series [7], [8]. In this method, when three capacitors are connected in series, the voltage of each capacitor becomes one-third. A similar method is also applied to inverters, i.e., multilevel inverters. As the capacitors are connected in series,the voltage of the devices is reduced when several devices are connected in series. Applying a multilevel inverter to EVs is proposed in [5] and [6]. A multilevel inverter can reduce the device voltage and the output harmonics by increasing the number of output voltage levels. There are several types of multilevel inverters: cascaded H-bridge (CHB) neutral point clamped flying capacitor and others . In particular, among these topologies, CHB inverters have been focused because of their modularity and simplicity . Various modulation methods can be applied to CHB inverters. CHB inverters can also increase the number of output voltage levels easily by increasing the number of H-bridges. However, if the number of output voltage levels is increased, the number of switching devices is also increased, which makes a multilevel inverter more complicated.

II. CIRCUIT TOPOLOGY

Fig.1 shows the circuit configuration of the generalised cascaded H bridge multilevel upper inverter.

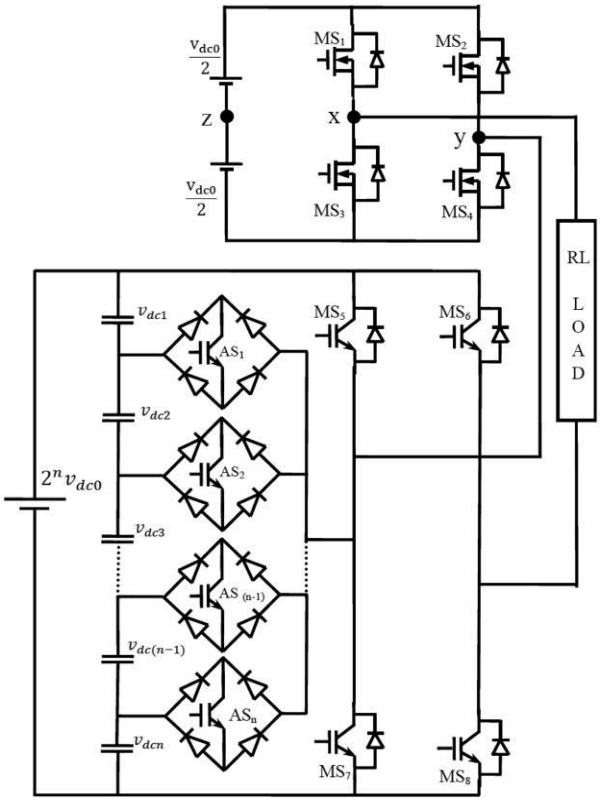


Figure 1 *Proposed Cascaded H-Bridge Multilevel Inverter In General*

Capacitor sources are connected in series manner. The auxiliary switches are connected in such a manner that it produces 11 levels of output with 2 auxiliary switches.When the number of levels increase at the output, the auxiliary switches used also increases. For every 4 level of increase at the output there is increase of only one auxiliary switch added to the circuit. It enhances the performance of the circuit without using more additional switches. When the number of levels at the output is 11 the number of switches used is 6 in the lower level inverter. When the number of levels at the output is 15the number of switches used is 7 in the lower level inverter. When the number of levels at the output is 19 the number of switches used is 8 in the lower level inverter. Hence the number of switches required in the inverter is reduced. At the upper level inverter totally only 4 switches are used at any levels. The capacitors used in the inverter causes voltage balancing problem. Hence dc-dc boost converter is required. Only two dc sources are required. One for upper inverter and other for lower inverter.

III. AVOIDANCE OF VOLTAGE BALANCING

PROBLEM

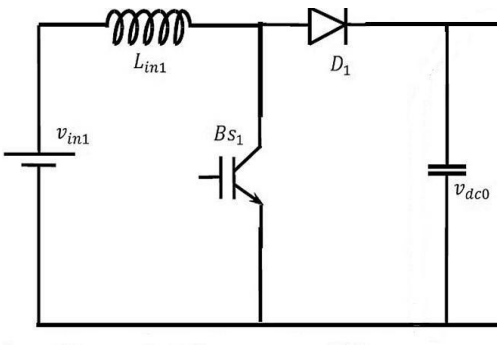


Figure 2 *Booster circuit*

Multi Output Boost (MOB) DC– DC converter as shown in figure 2 is the circuit used for advancing and regulating the low input voltage of dc to high input voltage which is fed to the inverter to produce ac voltage output. It is used

1. for boosting low voltages
2. balancing the capacitors at higher levels

DC-DC Boost Converter

The most basic type of boost converter consists of very few parts and is very straightforward. This type of converter charges an inductor with current flow while the switch is closed, and uses that current when the switch is opened to produce a voltage across the load that is higher than the initial voltage applied to the inductor. A filter capacitor across the output keeps the voltage from dipping too low across the load while the inductor is charging, and a diode ensures that the capacitor does not discharge itself across the switch when it is closed. The theory is that if one can open and close the switch fast enough, the load will see a apparently constant voltage that is boosted to some degree compared to the original voltage applied to the circuit. The ratio of output to input voltage depends on the duty cycle of the switch opening and closing, with higher ratios stirring with higher duty cycles. Many applications call for high step-up DC-DC converters that do not require isolation. Some DC-DC converters can provide high step-up voltage gain, but with the penalty of either an extreme duty ratio or a large amount of circulating energy. DC-DC converters with coupled inductors can provide high voltage gain, but their efficiency is degraded by the losses associated with leakage inductors. Converters with active clamps recycle the leakage energy at the price of increasing topology complexity. A family of high-efficiency, high step-up DC-DC converters with simple topologies is proposed. The proposed converters, which use diodes and coupled windings instead of active switches to realize functions similar to those of active clamps, perform better than their active-clamp counterparts. High efficiency is achieved because the leakage energy is recycled and the output rectifier reverse-recovery problem is alleviated.

IV.INTERNAL ARCHITECTURE EMBEDDED IN FPGA

VHDL code is used to model all module and Xilinx software is used as the design tools and to create reference waveforms too. The modulation and gate-drive control logic are implemented on a field-programmable gate array (FPGA), which is a powerful cost-effective solution. It allows complex logical and control algorithms, fast speed, and multiple input/output pins, which becomes particularly attractive for multilevel-converter control. The PWM logic has been modified for better performance and FPGA implementation. A simple approach is presented showing that current balance can be provided by adapting a well-known PWM strategy while minimizing switching speed using a novel sequential machine design. Finally, a prototype is built to obtain experimental results that validate the proposal. The experimental setup has been designed as a small-scale prototype of a high-current medium-voltage inverter. Each module has been planned with a modular structure. The hardware of the whole inverter has been carefully designed to avoid differences among the modules. Each switch has an independent low power supply for isolated firing of its gate. The layout of the drive circuits has been constructed with physical and electric symmetry so that the firing signals of the IGBT have no more than 10-ns difference in a module and among modules.

V. DC-DC BOOSTER CONVERTER TOPOLOGY

Guiding Principle for analysis: $\langle V_L(t) \rangle = 0$

When Switch is ON: $V_L(t) = q(t)[V_{in}]$

When Switch is OFF: $V_L(t) = (1-q(t))[V_{in} - v_{out}(t)]$

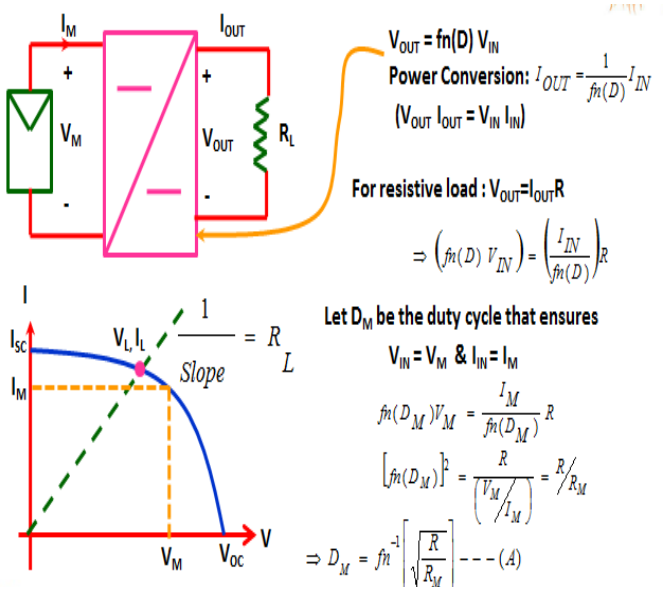
$$V_L(t) = q(t)[V_{in}] + (1-q(t))[V_{in} - v_{out}(t)]$$

Since C is very large $v_{out}(t) = V_{out} = Const.$

$$\langle V_L(t) \rangle = \langle q(t)[V_{in}] + (1-q(t))[V_{in} - V_{out}] \rangle = 0$$

$$\Rightarrow \langle q(t) \rangle V_{IN} + \langle (1-q(t)) \rangle [V_{IN} - V_{out}] = 0$$

$$\Rightarrow DV_{IN} + (1-D)[V_{IN} - V_{out}] = 0$$



VI. RESULTS

The gate driving signal is developed by using field programmable gate array (FPGA)-Xilinx SPATRAN 3A DSP. The software used to develop programs for SPATRAN 3A DSP are Xilinx ISE Design Suite and Multisim. Fig.3 shows the output waveforms of upper inverter and lower inverter with switching devices switched in various forms to produce multi level output. Figure 4 shows the final sine wave with 15 level output obtained by cascading upper level inverter and lower level inverter. The two level output and multilevel output are combined together to get the final sine wave. THD calculation for 15 level sine wave is obtained as shown in figure 5by selecting 3 cycles of the final output waveform. The THD calculated is about 7.97% which is low value compared to existing method. Due to this advantage failure of the devices can be minimized to certain amount. Table 1 shows the comparison of various parameters.

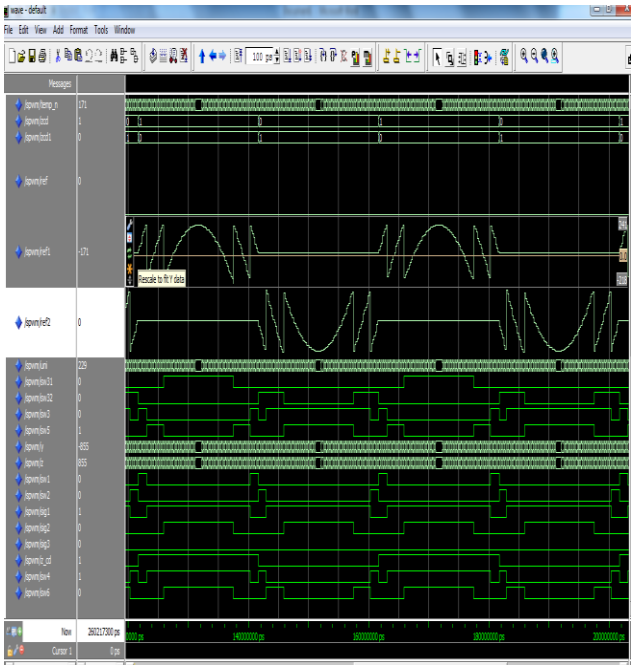


Figure 3 *Reference Waveform for Upper and lower Inverter*

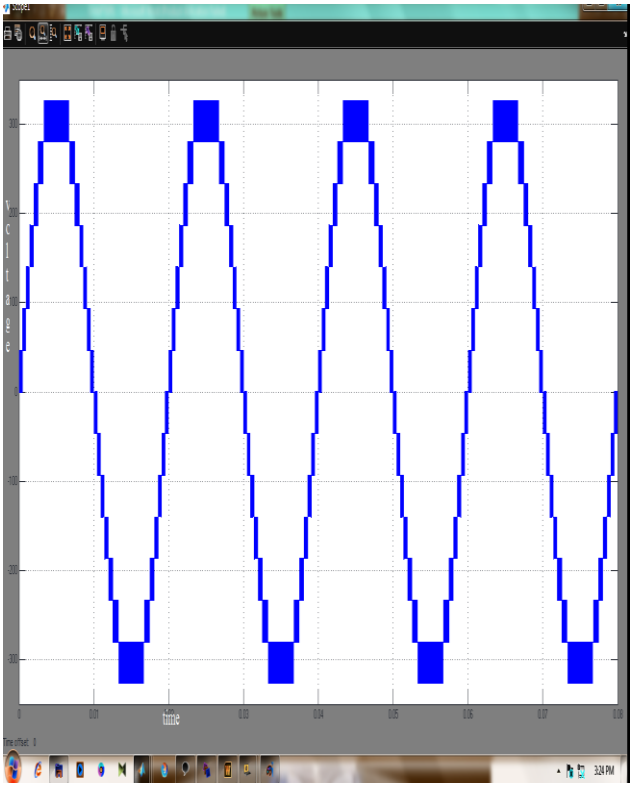


Figure 4 *Output waveform of cascaded upper and lowerInverter*

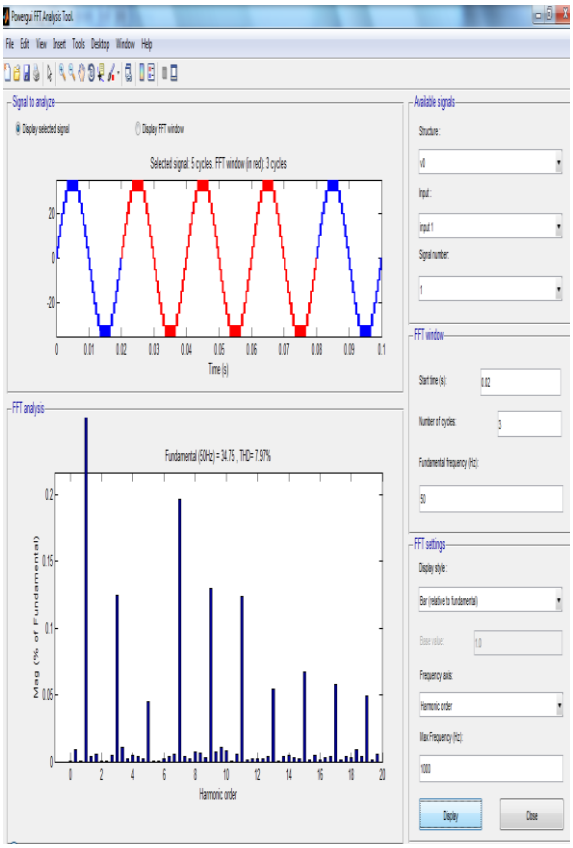


Figure 5 *THD Calculation*

Table 1 Comparison of various parameters

METHODS	LEVELS	NUMBER OF SWITCHING DEVICES USED	THD
EXISTING	15	14	11.6%
PROPOSED	15	10	7.97%

VII. CONCLUSION

Multilevel inverters offer enhanced output waveforms with minimum THD. This paper presents a novel single-phase multilevel inverter with reduced switching devices. Simulations are carried out in MATLAB/Simulink and implemented in real-time using FPGA board. The capacitor voltage balancing problem is avoided for higher levels by using booster circuit DC-DC converter. The proposed inverter can reduce the number of switching devices compared with conventional multilevel inverters in the same number of output voltage levels. The proposed inverter can also reduce the THD of its output waveform. In the proposed inverter, switching devices designed for low-voltage high-frequency operation and high-voltage lowfrequency operation.

VIII. REFERENCE

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