A Review On Design And Analysis Of D Flip Flop With Different Technologies

Hardeep Kaur, Sukhdeep Kaur, Er. Poonam Rani

M.tech student,Dept.ECE, Baba Farid college of Engineering & Technology, Bathinda, Punjab, India
M.tech student,Dept.ECE, Baba Farid college of Engineering & Technology, Bathinda, Punjab, India
Assistant Professor, Dept. ECE, Baba Farid college of Engineering & Technology, Bathinda, Punjab, India

Abstract: The Field of Digital Electronics have been directly towards to the low power of digital system. Recently the requirement of Probability and the improvement in battery performance indicate power dissipation is one of the most critical design parameter. wide utilization of memory storage systems and sequential logic in modern electronics triggers a demand for high performance and low area implementations of basic memory component one of the most state holding element is D flip flop. Here the proposed work is to design and analyze the D flip flop using CMOS, GDI technique, DETFF and CNTFET techniques and then compared with each other for power dissipation. The whole process of design and analysis of D flip flop and simulation will be done by using Tanner EDA.

Keywords: Flip flop,CMOS,GDI,DETFF ,CNTFET, Power disipation

I. INTRODUCTION

Now a days, Technology and speed are always moving forward, from low scale integration to large scale integration. So the power management has become a major issue in the development of a digital system. The major problem in power management is power dissipation. This paper proposed to present an approach to minimize the power consumption in flip flop design. The D flip flop can be considered as a basic memory cell or basic element for storing information. Flip flop is one of the most power consumption component. It is important to reduce the power dissipation in flip flops. In this paper a d flip flop design is proposed by comprehensive modeling of existing designs and using different Techniques as CMOS, GDI and CNTFET and compared with each other for power consumption, area and delay. The D flip flop designed in 180nm, 90nm and 65 nm technologies and simulation and comparison is done using Tanner EDA and performance parameters like power, delay will analyzed and compared with all the designs.

II. DESCRIPITION OF D-FLIP FLOP

The D flip flop is an important part of the Modern digital circuit. It is an electronic circuit that stores a logical state of one or more data input signals in response to a clock pulse. D flip flop is generally called the data flip flop. It is also called Delay flip flop. It will just pass the data given into the input to the output. The data will move from input to output only if the clock signal is arrived.(either negative edge of the clock or positive edge of the clock)and delays it by one clock cycle. The basic structure of DFF and its timing diagram Responses explain below in Figure.1 &2.

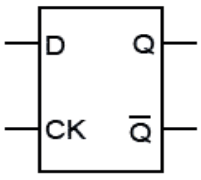

Fig.1.*Graphical symbol of DFF*

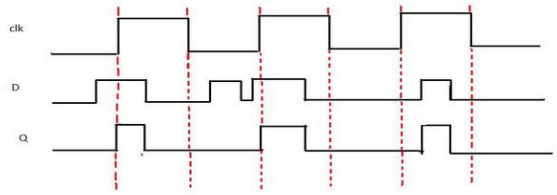

Fig.2 *Timing Response of basic DFF*

The working of D flip flop is similar as d Latch except the output of the D Flip flop takes the state of the D input at the moment of a positive edge at clock pin or the negative edge if the clock input is active low and delayed it by one clock cycle. The storage element is major power consuming component in VLSI system. Hence this paper all three major concerns of VLSI system, the power consumed, delay and area consumption are concentrated.

III. LITERATURE REVIEW

Vladmir stojanovic and vojin G. oklobdzija has proposed a set of rules for consistent estimation of real performance and power features of flip flop and master slave structures. The analysis approach reveals the sources of performance and power consumption in different ;logic styles. They proposed the comparative analysis of master slave latches and flip flips and their suitability of different logic styles for high performance and low power systems. Arkadiy morgenshtien .et.al has introduced a new technique of low power digital circuit design that is GDI(Gate diffusion input) Technique. Which allows reducing power consumption, propagation delay, and area of the digital circuit while maintaining low complexity of logic design. In this a low voltage dual pulse clock double edge triggered d flip flop is proposed. In this the transistor count is reduced by 40% and power dissipation is reduced by 21% to 36% than other methods using o.35um technology. Arkadiy Morgensthien .et. al have designed an efficient d flip flop using GDI technique. This DFF design allows reducing power delay product and area of the circuit. In this the circuit is implemented using 0.35um and 0.18um technologies. To compare with other conventional methods in this 45% reduction in power delay product. M.W.phyu. et.al has proposed a low power and high speed flip flop. The

proposed flip flop has no precharging and utilizes conditional discharging in the dynamic stage to derived its enhancement. Simulation results derived from 0.18um cmos technology. In this 13% improvement in total gate area for minimum power delay product. Fatemeh Aezinia.et.al they proposed a novel low power flip flop circuit. This circuit is applied in two cases single edge triggered or double edge triggered. This leads to lower delay and power dissipation. Circuits are simulated using HSPICE 180nm technology. it shows the new circuit have better speed than others. Yu Chien-Cheng has proposed a double edge triggered flip flop suitable for low power applications. This circuit has less transistor count and it consumes less power than other methods. Manoj sharama,Dr Aarti noor.et.al have designed a single edge triggered static D flip flop which is suitable for low Area requirements. The flip flop is implementing using 0.6 micron technology. In this the transistor count is less than any other existing SETDFF and has a high percentage reduction in power. Jin-fa lin ,Ming-Hwa sheu et.al have designed a dual mode pulse triggered FF which is supporting the functional versatility .in this combination of the pulse generator and a level sensitive latch is used. It performs full voltage swing operations. Wing-shan Tam et.al has proposed a double edge triggered half static clock gated D type flip flop. In this a clock gating circuit is used to achieve better race tolerance circuit compactness and energy efficiency without the use of pulse generator. This circuit is designed by using 0.18um technology. it shows 96% reduction in redundant power. Manish sharama.et.al has proposed a modified single edge triggered D flip flop for low power applications. In this design comparison is done using 65nm and 45nm technologies. It is suitable for portable applications. N. Vishnu vardhan reddy .et.al have designed a sub threshold low power d flip flop circuit based on GDI technique. It allows reducing power consumption, delay and area of the digital cicuit.sub threshold operation is suited for circuits which have low frequency requirements. Amit grover and Smer singh has explains a new implementation of efficient D flip flop using GDI technique, Power PC,DSTC and HLFF .this design allows reducing power delay product area of the circuit. The performance is carried out by HSPICE simulation with180nm &90nm technologies. Jin-fa Lin have designed an explicit type pulse triggered structure and modified true single phase clock latch based on a signal feed through scheme. It solves the long discharging path problem. The simulation is done using 90nm technology. Seyed E.Esmaeili,Asim j .et.al has introduced a new flip flop for use in a low swing LC resonant clocking scheme. This enables 6.5%reduction in power compared to full swing flip flop. The functionality of the proposed flip flop is tested and verified by using 90nm CMOS technology. It achieved 5.8% reduction in total power with 5.7% area overhead. M. Guru santhana Bharati, P.Nagarajan has proposed a single edge triggered and a double edge triggered logic module flip flops. That is implemented by using Tanner EDA and compared using 0.25um & 0.18um CMOS VLSI Process and 0.18nm TSMC VLSI process. It shows9.11% improvement in power. It is well suited for modern low power VLSI system design. Priya jose has introduced a proposed P FF design used two new design measures. The first one successfully reduces the number of transistors stacked along the discharging path by incorporating a PTL based AND logic. The second one supports conditional enhancements to the height and width of the discharging pulse so that the size of the transistors in pulse generation circuit can be minimum. The power consumption of this design is the lowest because of shorter discharging path. R dhivya bharathi & M sunil Karthik has proposed a pass transistor based D flip flop design using negative edge triggered circuit.the simulation is done using Tanner EDA and using 130nm technology. It saves up to 85% power and 40% improvement in area constraints when compared with other methods. This can be much suited for application of battery oriented operation for less power and area. A.vinodhimi .et .al has enumerates low power high speed design of linear feedback shift register using D flip flop. It shows a design of D flip flop using two different logic styles to increase the overall speed of the system. In this LSFRs using transmission gates and pipe logic are presented. The power consumption and dissipation is reduced by reducing the number of transistors and time consumption.

IV. INTRODUCTION ABOUT TECHNOLOGIES

CMOS Technology (Complementary metal oxide semiconductor)- CMOS is a technology used for constructing integrating circuits. CMOS technology is used in microprocessors, microcontrollers and other digital logic circuits. CMOS refers to both a particular style of digital circuitry design and the family of processes used to implement that circuitry on integrated circuits. CMOS circuitry dissipates less power than logic families with resistive load. CMOS circuit use a combination of P type and N type metal oxide semiconductor field effect transistors to implement logic gates or other digital circuits. The transistors arranged in a structure formed by two complementary networks. In this pull up network is complement of pull down. CMOS circuits are constructed in such a way that all PMOS transistors must have either an input from the voltage source or from other PMOS transistor. Similarly all NMOS transistors must have either an input from ground or from other NMOS transistors. CMOS accomplishes current reduction by complementing every nMOSFET with a pMOSFET and connecting both gates and drains together.this arrangement greatly reduces power consumption and heat generation. A static CMOS inverter shown in figure 3.

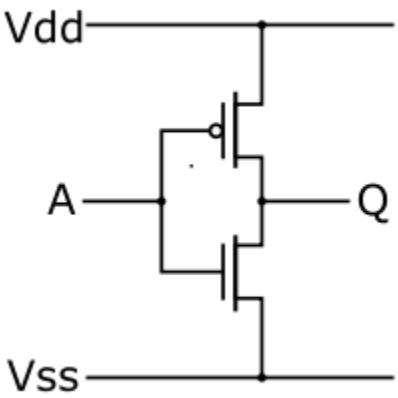

Fig.3 *Static CMOS inverter*

The power supplies for CMOS are called Vdd or Vss or Vcc and GND (Ground) depends upon manufacturer. An important characteristic of a CMOS circuit is the duality that exists between its PMOS transistor or NMOS transistors. GDI

Technology (Gate Diffusion Input)-GDI technique is a novel technique for low power digital circuit design.GDI technique helps in designing low power digital circuit by which the demerits of other methods has been eradicate. This technique allows reducing power consumption, power delay and area of the digital circuit. The GDI method based on a simple logic cell that is shown in figure 4.

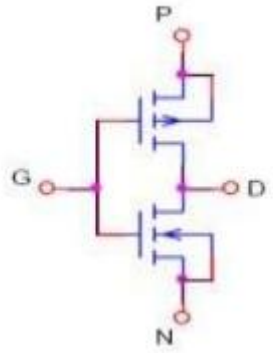

Fig.4 *Basic GDI Cell*

GDI cell contains four Terminals in which it has three inputs G (common gate input of PMOS and NMOS), P (input of the source/drain of PMOS), N(input of the source/drain of NMOS) and one output D. The source of PMOS in a GDI cell is not connected to Vdd or source of NMOS is not connected to Gnd.this feature gives two extra inputs to GDI cell to make design more flexible. Some functions performed by basic GDI cell are shown in Table.1.

N	P	G	D	FUNCTION
'0'	B	A	$A\overline{B}$	F1
B	1	A	$A+\overline{B}$	F2
'1'	B	A	A+B	OR
B	O	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	1	A	$\overline{A}$	NOT

Table.1 *Functions of Basic GDI cell*

The GDI functions given in Table .1 are simply the extension of single input CMOS inverter structure into triple input GDI cell. This makes GDI cell suitable for implementation of any logic function. CNTFET Technology (Carbon nanotube field effect transistor)-CNTFET refers to a field effect transistor that utilizes a single carbon nanotube or an array of of the nanotubes as a channel material instead of bulk silicon. The carbon nanotube field effect transistor is three terminal device similar to MOSFET. The CNTFET has been advocated as one of the possible alternatives to replace the conventional MOSFET due its excellent performance characteristics. In CNTFET the carrier velocity is almost double due to high mobility on account of ballistic transport operation. It utilizes a SWCNTs(single wall carbon nanotube) as a channel material. SWCNT is a nanotube formed by single sheet of graphite. It can either be metallic or semiconducting depends on the chirality vector. In a CNTFET the number of CNTs is changed because a CNTFET uses CNTs as a conducting channel between the source and drain. The width of CNTFET increase when the number of CNTs in a CNTFET is increased. The electrons in a carbon nanotube are confined to the atomic plane of the graphene. The electrons can only move along the axis of the tube. Figure 5&6 shows the structure, top view and cross section view of CNTFET.

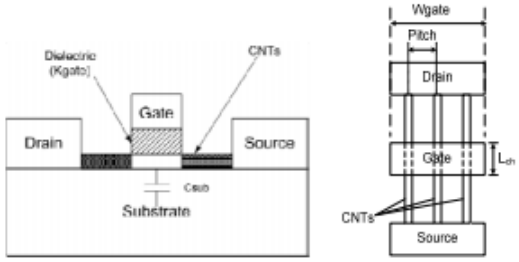

Fig.5 *Structure of CNTFET and Top view*

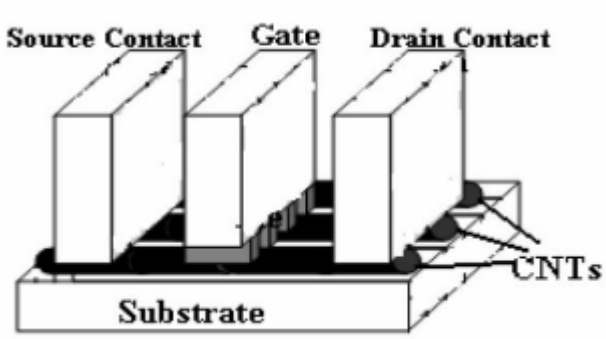

Fig.6 *Cross Sectional view of CNTFET*

The diameter of CNT can be calculated based on the following.

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + mn}$$

Where a0 is the inter atomic distance between each carbon and its neighbor. The importance of CNT diameter is that it determines the band gap energy of the tube. The following relation expresses the SWCNT band gap energy.

$$E_{gap} = 2Y_{0\,c-c} / d$$

Where E gap is the band gap and Y0 is the carbon to carbon distance and d is the diameter of the nanotube. As d gets larger the band gap smaller and the nanotube becomes more conducting. CNTFETs provides a unique opportunity to control threshold voltage by changing the chirality vector or the diameter of the CNT. The channel width of the CNTFET depends upon the number of CNTs and pitch value which is the distance between the centers of two adjoining CNTs under the same gate. Its approximate value can be determine using following equation.

$$W \approx \min(W_{\min}, N \times S)$$

Where Wmin is the minimum gate width, N is the number of tubes and S is the pitch. By using CNTFET speed and power w.r.t CMOS is achieved better.

V. CONCLUSION

In this paper different technologies are proposed to design a D flip flop for low power and high performance systems. And related work also discussed .Using these technologies Design and analysis of D flip flop will be done and a comparison and simulation will be done using Tanner EDA. The proposed D FF will best suited for low power applications and power consumption and area can be also reduced.

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