# A Miller Compensated Gain & Phase Enhanced Two-Stage Differential OTA's Using Positive Feedback At Differential Stage

**[1]Raghavendra Gupta,[2]Prof. Sunny Jain**

[1] M.Tech Research Scholar, Dept. ECE, Lakshmi Narain College of Technology, RGPV University, Bhopal, Madhya Pradesh, India.
[2]Assistant Professor, Dept. ECE, Lakshmi Narain College of Technology, RGPV University, Bhopal, Madhya Pradesh, India.
Emails: [1]theraghav.india@gmail.com, [2]sunnyjain2008@gmail.com

**ABSTRACT**: Miller compensated OTAs are generally used for frequency stabilization. With increasing in gain of cascaded OTA the frequency response decreases in terms of gain bandwidth product and phase margin. To increase the gain at differential stage of OTA, a positive feedback is applied which increases gain without decreasing the gain bandwidth product and phase margin. The above prototype is implemented on 65 nm CMOS IBM technology in LT spice using spic model.

**INDEX TERMS:** CMOS technology, Operational Amplifier, Operational Trans-conductance Amplifier (OTA), Gain Bandwidth Product (GBW), Phase Margin, Positive Feedback, Gain Enhancement.

## I. INTRODUCTION

Wireless technology generally uses OTA in every base circuit of wireless network, At high frequencies the operational amplifier does not perform well hence OTA are used. The demand of high-speed, large data rate are increasing day to day and the scaling down of CMOS technology produces the challenges for analog and digital circuit in terms of frequencies stabilization and gain. OTA uses feedback for their stabilization, and high gain is the requirement for the large data rate and frequency stableness of the operational transconductance Amplifier circuits, So same with high DC gain is obtained by cascading the gain stages or by cascoding of the gain stages. As the advancement in technology and the reduction in power supply reduces the gain of stages at such supply is hard to achieve [1],[2],[6]. Out of Different compensation techniques that are used for frequency stabilization, the Miller compensation is the most universally adopted compensation technique. It is based on pole splitting method. In this method the frequency of first pole decreases and the other pole frequency increases, such that the gain versus frequency curve crosses the 0db line in between the first pole and other poles. The propagation to Miller compensation is raised phase compensation which improves the 3db bandwidth, it uses positive feedback RC cross-linked at second gain stage, to enhance the gain and increases the frequency response [1],[3],[4].

In this paper, a positive feedback at differential stage of OTA is used, which increases only the Trans-conductance of differential stage without affecting the frequency response of the OTA. The robustness of this proficiency is assessed by stimulating the circuit at various temperatures in 65 nm CMOS technology for different capacitive loads.

## II. AMPLIFIER COMPENSATION

### 1. Miller compensation

A conventional Miller compensated two-stage OTA is shown in figure 1 where $R_M$ & $C_M$ are the Miller compensated resistance and capacitance, the small signal how model is shown in figure [1],[2]. $C_{01}$ & $r_{01}$ is the capacitance and resistance of first stage of OTA and $g_{m1}$ is the transconductance of first stage. $C_{02}$ & $r_{02}$ is the capacitance and resistance of second stage of OTA with $g_{m1}$ is its trans-conductance , $C_L + C_{02} \approx C_L$ as $C_2$ is very large. The approximate expression for pole and zero are shown below from equation [2].

$$Z_1 \approx \left((g_{m2}^{-1} - R_M)C_M\right)^{-1}$$
$$P_1 \approx (-g_{m2}r_{02}r_{01}C_M)^{-1}$$
$$P_2 \approx -g_{m2}(C_L)^{-1}$$
$$P_3 \approx (C_M R_M)^{-1}$$

The first pole P1 is at low frequency which set the GBW of the OTA, the zero $Z_1$ cancel out $P_2$ with $C_L$ and $P_2$ &$P_3$ are very far-off from P1, so P1 will be the dominant pole to stabilize the frequency, when $C_L$ is not fixed then the compensated capacitor $C_m$ will be used for charging and discharging of output load, the worst case arises for high capacitive load of OTA which reduces the frequency response [12]. This unfortunately reduces the GBW and other drawback of such compensation is the process variation.

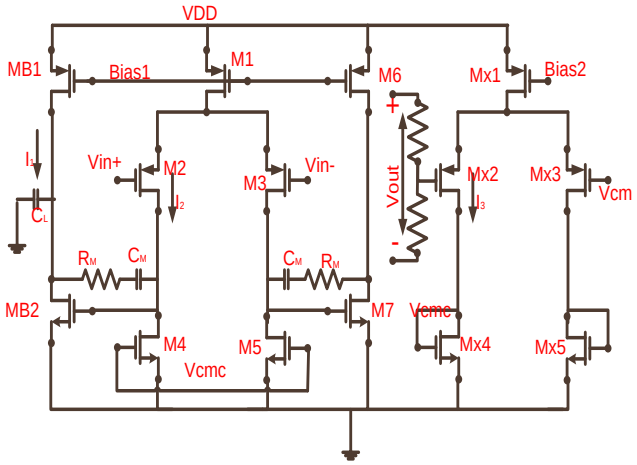


***Figure.1*** *Miller Compensated Two-Stage OTA.*

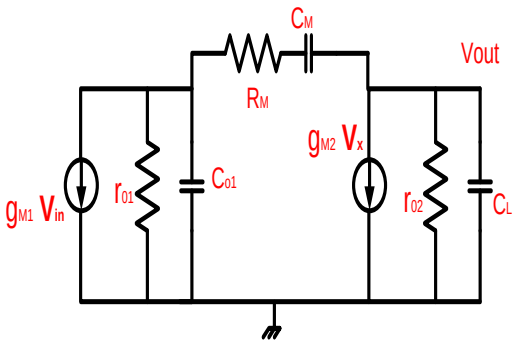


***Figure.2*** *Small Signal Model of Miller Compensated Two-Stage OTA.*

## 2. Enhancement phase compensation

It is clear that Miller compensation improves the phase margin by reducing gain bandwidth, If we try to increase the gain, it reduces the phase margin and made the pole complex [3],[4]. A positive feedback at the output gain stage increases the gain bandwidth based on this approach enhanced phase compensation work as shown in figure 3. When two zero are introduced by positive feedback using register and capacitor, this will increase a pole also, to make it fourth order transfer function. But due to Miller dominant pole condition two zero cancel out to polls to make it second order transfer function. Small signal model is shown in figure 4. The RC cross-linked couple are made to increase the gain of the buffer and to stabilize it the transfer function of the buffer is given by the following equations given below [1], and pole and zero approximated from the transfer function, as it is seen that the DC gain of the OTA is unchanged as RC link the present an open circuit using KCL and KVL.

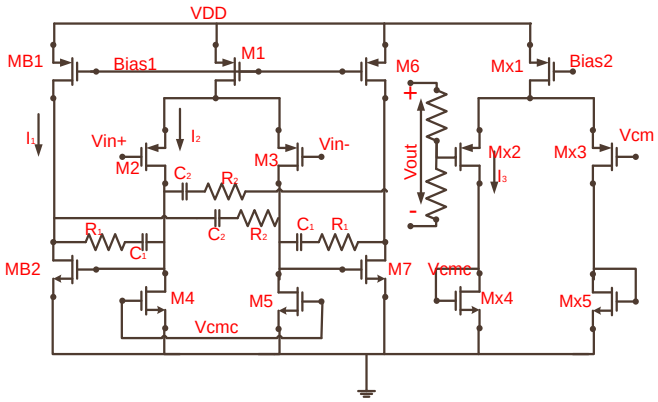


***Figure.3*** *Phase Enhanced Compensated Two-Stage OTA.*

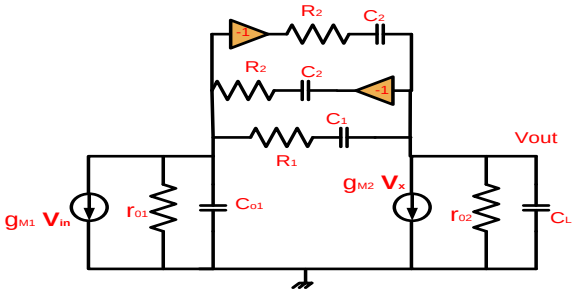


***Figure.4*** *Small Signal Model of Phase Enhanced Compensated Two-Stage OTA.*

$$\frac{V_{out}}{V_{in}} = g_{m1}g_{m2}r_{01}r_{02}\frac{(g_{m2}^{-1}(C_1C_2R_1 - C_1C_2R_2) + R_1R_2C_1C_2)S^2 + (g_{m2}^{-1}(C_2 - C_1) + C_1R_1 + C_2R_2)S + 1}{(C_{01}C_LC_1C_2r_{01}r_{02}R_1R_2)S^4 + D_1S^3 + D_2S^2 + D_3S + 1}$$

$$D_1 = C_{01}C_LC_1r_{01}r_{02}R_1 + C_{01}C_LC_2r_{01}r_{02}R_2 + C_{01}C_1C_2r_{01}r_{02}R_1 + C_LC_1C_2r_{01}r_{02}R_1 + C_{01}C_1C_2r_{01}r_{02}R_2 + C_LC_1C_2r_{01}r_{02}R_2 + C_{01}C_1C_2r_{02}R_1R_2 + C_LC_1C_2r_{01}r_{02}R_1$$

$$D_2 = C_{01}C_Lr_{01}r_{02} + C_{01}C_2r_{01}r_{02} + C_LC_1r_{01}r_{02} + C_{01}C_2r_{01}r_{02} + C_LC_2r_{01}r_{02} + C_{01}C_1r_{01}R_1 + C_LC_1r_{02}R_1 + 4C_1C_2r_{01}r_{02} + C_{01}C_2r_{01}R_2 + C_LC_2r_{02}R_2 + C_1C_2r_{01}R_1 + C_1C_2r_{02}R_1 + C_1C_2r_{01}R_2 + C_1C_2r_{02}R_2 + C_1C_2R_1R_2 + C_{01}C_LC_1C_2r_{01}r_{02}R_2g_{m2} - C_{01}C_LC_1C_2r_{01}r_{02}R_1g_{m2}$$

$$D_3 = C_{01}r_{01} + C_Lr_{02} + C_1r_{01} + C_1r_{02} + C_2r_{01} + C_2r_{02} + C_1R_1 + C_2R_2 + g_{m2}C_1r_{01}r_{02} - g_{m2}C_2r_{01}r_{02}$$

$$Z_1 \approx -\frac{1}{C(R_1 + R_2)}$$

$$Z_2 \approx -\frac{R_1 + R_2}{C(R_1R_2)}$$

$$P_1 \approx -\frac{1}{(C_L + 2C)r_{02} + 2Cr_{01}}$$

$$P_2 \approx -\frac{(C_L + 2C)r_{02} + 2Cr_{01}}{2C_Lr_{02}r_{01} + 4r_{02}r_{01}C^2}$$

$$P_3 \approx -\frac{2C_L + 4C}{CC_L(R_1 + R_2)}$$

$$P_4 \approx -\frac{R_1 + R_2}{C_{01}(R_1R_2)}$$

$$R_1 + R_2 \approx \frac{2C_L r_{02} r_{01} + 4C r_{02} r_{01}}{C_L r_{02} + 2C(r_{02} + r_{01})}$$

$$\alpha/(1+\alpha)^2 \approx \frac{C_L}{2C_L + 4C}$$

$$BW_{RATIO} \approx \frac{(C_L + C_M) r_{02} + g_{m2} r_{02} r_{01} C_M}{(C_L + 2C) r_{02} + 2C r_{01} + C(R_1 + R_2)}$$

$$\boldsymbol{GBP_{RATIO} \approx \frac{(R_1 + R_2) C_L}{C_{01} R_1 R_2 g_{m2}}}$$

## III. MILLER-COMPENSATED ENHANCEDGAIN AND PHASE COMPENSATION

Fig. 5 shows a configuration of diff-amp circuit using positive feedback with integrated resistors. The circuit does not limit the output voltage drop or swing, due to the absence of the vertical stacking cascode structure or the MOSFET diode-connected circuit [16].

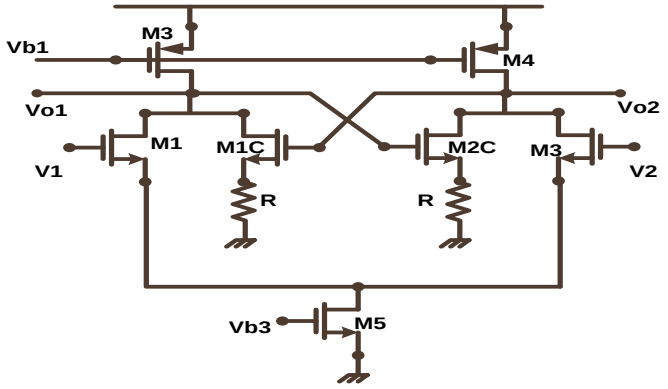


***Figure.5*** *Gain Enhancement Differential Amplifier Using Positive Feedback at Differential End.*

The cross-coupled MOSFETs provide the positive feedback to the output nodes with a negative transconductance, -$g_m$, which brings down the positive output resistance of both PMOS and NMOS loads of diff-pair circuit. As a result, the cross-coupled MOSFET increases the amplifier gain. The transfer function of small-signal gain is written as,

$$A_d = \frac{V_{02} - V_{01}}{V_{id}} = \frac{g_{m1}}{\left(\frac{1}{r_{01}} + \frac{1}{r_{03}} + \frac{1}{R_o} - G_M\right)}$$

Where$r_{01}$and $r_{03}$ are the output resistance of M1 and M3. The output resistance, $R_0$, can be written as

$$R_0 = \frac{V_t}{i_t} = r_{o1c} + R + (g_{m1c} + g_{m1be}).r_{01c}\,R$$

where$r_{o1c}$ ' $g_{m1c}$ ' and $g_{m1be}$ are the output resistance, transconductance , and body effect transconductance of $M_{1c}$ respectively. R is the integrated resistor. Thetransconductance $G_M$ can also be written as

$$G_m = \frac{r_{01c} g_{m1c}}{r_{01c} + R + (g_{m1c} + g_{mb1c}).r_{01c}\,R}$$

As we have seen that the positive feedback enhances the gain of differential pair without adding any extra stage. As we know the extra stages introduce the poles and makes the system higher order, then the previous order which inturn makes it unstable at high frequency.. It is clear from the above equations that using positive feedback at the differential is stage launched as the positive output resistance of both NMOS and PMOS of differential pair circuit as a result cross coupled MOSFET increases the gain. This technique is used in enhanced phase compensation to increase the gain of the operational tran-sconductance amplifier the schematic of the proposed circuit is shown in the figure 6. The proposed circuit increases the gain without affecting the phase margin. It only increases the DC gain of the proposed OTA using this technique. The transconductance of the first stage thus increases which increases the gain. The other important parameters of OTA is the slew rate in comparison to Miller compensation and enhanced phase compensation the proposed technique will improve the slew rate considerably this is due to enhanced phase and increasing gain of the OTA to get deep in slew rate behavior. In input stage current was decreased and output stage current was increased to get optimal slew rate as in [6],[7]. Where $I_2$& $I_1$ are the input and output current at two stages and are related as,

$$\mathbf{I_2 \approx 2I_1(1 + C_L/C_M)}$$

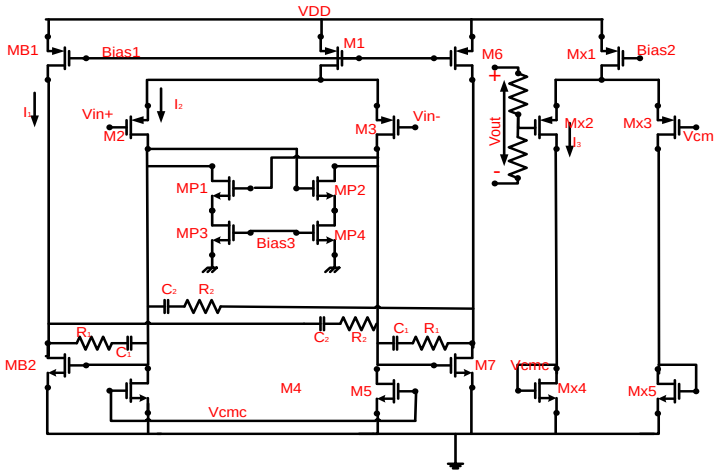


***Figure.6*** *Schematic of Proposed OTA With Gain And Phase Enhancement.*

## IV. SIMULATION RESULTS

The OTA stimulated in LT spice using 65 nm CMOS IBM technology with the BSIM-4 transistor model. The summation of the proposed compensation is compared with the conventional Miller compensation and the enhanced phase compensation, the performance comparison of the OTA is summarized in table 1 in terms of bandwidth, phase margin, power, and gain bandwidth product. Table 2 shows performance comparison in terms of slew rate of the proposed OTA. Table 3 shows summarized companies and report of the previous work with the recent work on OTA. Figure 7 shows the frequency response of the proposed OTA with different temperature which ranges from $-60^0$ to $120^0$, figure 8 to 9 shows gain and phase response to a different temperature points. Figure 10 shows the frequency response of the proposed OTA with different capacitive load ranges from 1p to 10p at $27^0$ temperatures. Figure 11 and 12 shows gain and phase response of the OTA at different capacitive loads. Figure 13 shows step response of the OTA for 1.2 voltage step size with time period of 200 ns for slew rate calculation at the rising and falling edge.

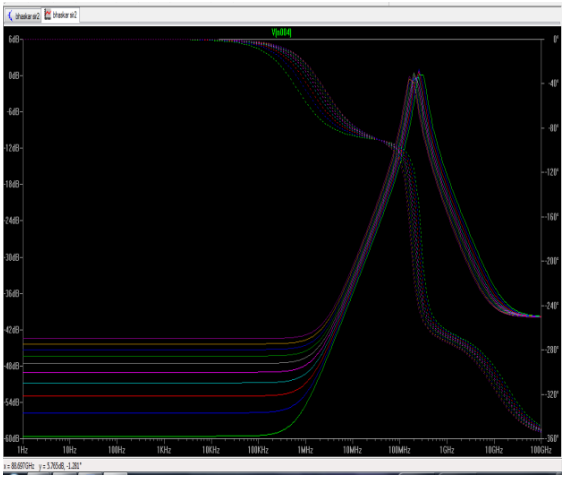

***Figure.7*** *Frequency Response of The Proposed OTA With Temperature Range From $-60^0$ to $120^0$.*

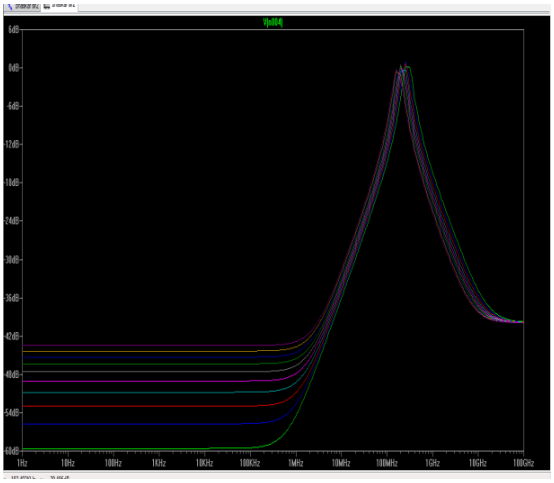

***Figure.8*** *The Gain versus Frequency Curve of The Proposed OTA With Temperature Range From $-60^0$ to $120.^0$*

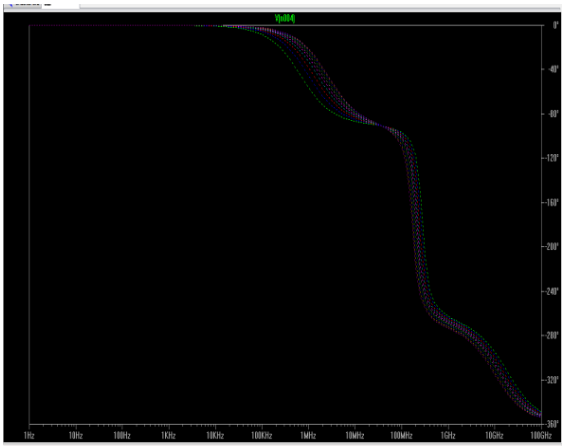

***Figure.9*** *Phase versus Frequency Curve of The Proposed OTA with Temperature Range From $-60^0$ to $120^0$.*

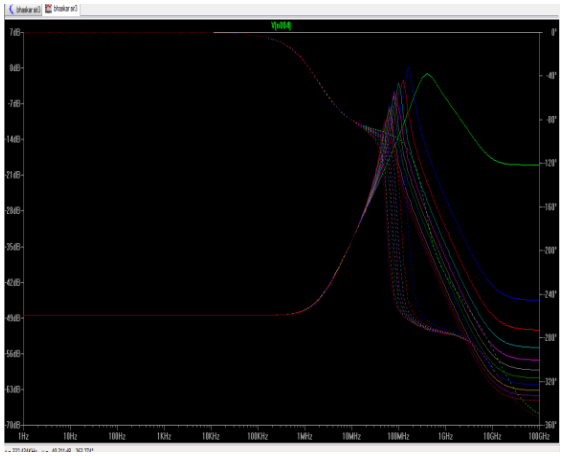

***Figure.10*** *Frequency Response of The Proposed OTA With Different Capacitive Load Ranges From 1p to 10p.*

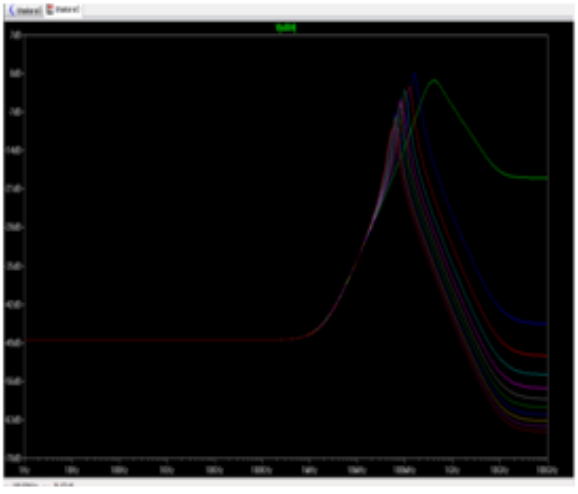

***Figure.11*** *Gain versus Frequency Proposed OTA With Different Capacitive Load Ranges From 1p to 10p.*

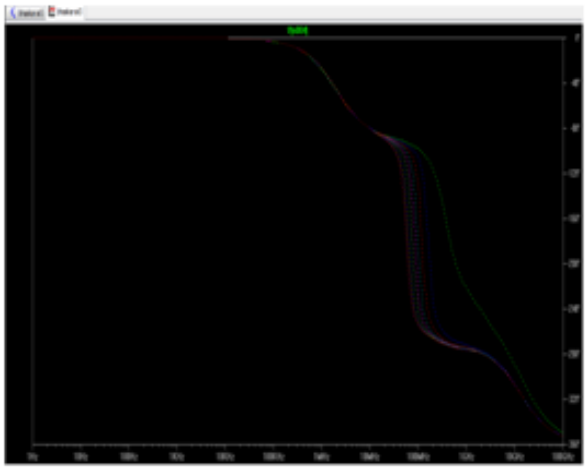

***Figure.12*** *Phase versus Frequency Proposed OTA With Different Capacitive Load Ranges From 1p to 10p.*

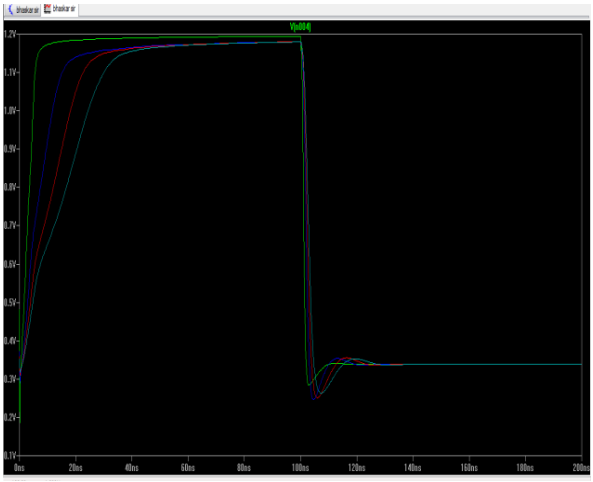

***Figure.13*** *Step Response of The Proposed OTA With Capacitive Load of 4p,6p,8p &10p For Slew Rate Calculation.*

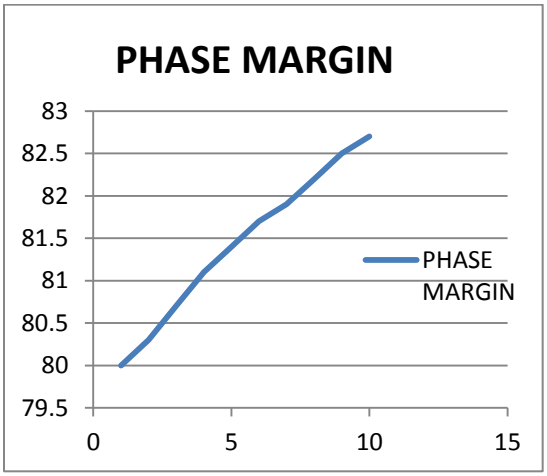


***Figure****.14 OTA Phase Margin versus Temperature with Enhanced Gain And Phase Compensation.*

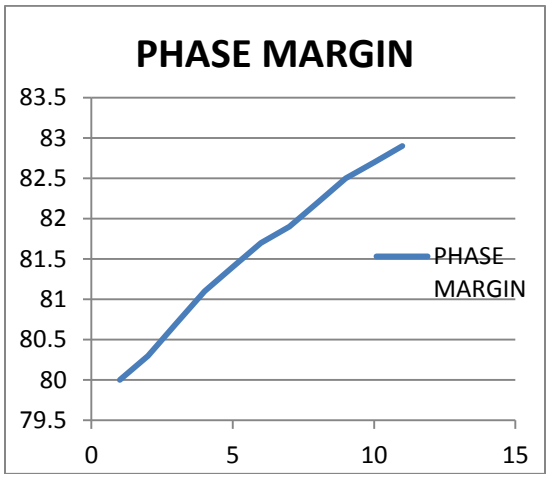


***Figure.*** *15 OTA Phase Margin versus Load Capacitance For Enhanced Gain And Phase Compensation.*

## *V. COMPARISONS TABLES*

| ***Parameter*** | ***Miller Compensation*** | ***Phase Enhancement Compensation*** | ***Miller Compensated Enhanced Gain & Phase*** |
|---|---|---|---|
| $BW_{3db}$(MH) | 3.67 | 11.38 | 10 |
| GBP(MHz) | 378 | 1050 | 2511 |
| Phase Margin | 43.2 | 50.7 | 86 |
| Power(mW) | .68 | .68 | .69 |
| Area $\mu m^2$ | 53 × 60 | 54 × 60 | NA |

***Table 1*** *Performance comparison of The OTA.*

| ***Compensation*** | ***Miller*** | ***Enhanced Phase*** | ***Miller Compensated Gain Enhanced Phase*** |
|---|---|---|---|
| $SR_{diff}$(V/µs) | 118.9 | 254 | 300 |
| $SR^{+}$(V/µs) | 63.2 | 118.8 | 154 |
| $SR^{-}$(V/µs) | 53.6 | 128.9 | 182 |

***Table 2*** *Slew Rate Comparison of The OTA.*

| *Para-meter* | *NCFF [9]* | *RFC [13]* | *FF [14]* | *GBCA [15]* | *SMC [10]* | *[1]* | *THIS WORK* |
|---|---|---|---|---|---|---|---|
| Technology | 500 | 180 | 1890 | 180 | 500 | 65 | 65 |
| Supply(V) | $\pm 1.25$ | 1.2 | 1.8 | 1.8 | 2 | 1.2 | 1.2 |
| Power | 15.8 | 1.44 | 0.2 | 3.8 | 0.38 | .75 | .69 |
| GBP | 300 | 134.2 | 1800 | 600 | 4.6 | 780 | 2511 |
| CL | 12 | 5.6 | .0045 | 1 | 120 | 1 | 10 |
| $SR^{+-}$ | NA | 94.1 | NA | 800 | 3.28,1.31 | 119,129 | 154,182 |

***Table 3*** *Comparison of The OTA with Previous Work.*

## VI. CONCLUSION

A two stage positive feedback gain and phase enhanced compensated technique is used which improves the gain bandwidth, gain, phase and slew rate of the OTA. This compensated OTA is the best suited for the wireless sensor network for high speed. The above technique of compensation is robust against temperature variation and load capacitance up to 10pf. This OTA is used efficiently for high-speed operation.

## REFERENCES

[1]. Mohammed Abdulaziz, Markus Törmänen and HenrikSjöland, IEEE "A Compensation Technique for "Two-Stage Differential OTAs" IEEE Transactions On Circuits And Systems, vol. 61, no. 8, august 2014.

[2]. M. Abdulaziz, A. Nejdel, M. Törmänen, and H. Sjöland, “A 3.4 mw65 nm CMOS 5th order programmable active-RC channel select filter forLTE receivers,” in Proc. IEEE RFIC, 2013, pp. 217–220.

[3]. P. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, Analysis and Design ofAnalog Integrated Circuits. Hoboken, NJ, USA: Wiley, 2010.

[4]. M. Vadipour, “Capacitive feedback technique for wide-band amplifiers,”IEEE J. Solid-State Circuits, vol. 28, no. 1, pp. 90–92, Jan. 1993.

[5]. A. Vasilopoulos, G. Vitzilaios, G. Theodoratos, and Y. Papananos,“A low-power wideband reconfigurable integrated active-RC filter with73 dB SFDR,” IEEE J. Solid-State Circuits, vol. 41, no. 9, pp. 1997–2008,Sep. 2006.

[6]. G. Palmisano, G. Palumbo, and S. Pennisi, “Design procedure for twostagecmostransconductance operational amplifiers: A tutorial,” AnalogIntegr. Circuits Signal Process., vol. 27, no. 3, pp. 179–189, May 2001.

[7]. K. N. Leung, P. K. T. Mok, W.-H. Ki, and J. K. O. Sin, “Three-stagelarge capacitive load amplifier with damping-factor-control frequencycompensation,” IEEE J. Solid-State Circuits, vol. 35, no. 2, pp. 221–230,Feb. 2000.

[8]. H.-T. Ng, R. M. Ziazadeh, and D. J. Allstot, “A multistage amplifiertechnique with embedded frequency compensation,” IEEE J. Solid-StateCircuits, vol. 34, no. 3, pp. 339–347, Mar. 1999.

[9]. B. Thandri and J. Silva-Martinez, “A robust feedforward compensationscheme for multistage operational transconductance amplifiers with nomiller capacitors,” IEEE J. Solid-State Circuits, vol. 38, no. 2, pp. 237–243, Feb. 2003.

[10]. X. Fan, C. Mishra, and E. Sanchez-Sinencio, “Single miller capacitorfrequency compensation technique for low-power multistage amplifiers,”IEEE J. Solid-State Circuits, vol. 40, no. 3, pp. 584–592, Mar. 2005.

[11]. H. Lee, K. N. Leung, and P. K. T. Mok, “A dual-path bandwidth extensionamplifier topology with dual-loop parallel compensation,” IEEE J. Solid-State Circuits, vol. 38, no. 10, pp. 1739–1744, Oct. 2003.

[12]. A. Grasso, G. Palumbo, and S. Pennisi, “Three-stage CMOS OTA forlarge capacitive loads with efficient frequency compensation scheme,”IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 10, pp. 1044–1048,Oct. 2006.

[13]. R. Assaad and J. Silva-Martinez, “The recycling folded cascode: A generalenhancement of the folded cascode amplifier,” IEEE J. Solid-StateCircuits, vol. 44, no. 9, pp. 2535–2542, Sep. 2009.

[14]. N. Krishnapura, A. Agrawal, and S. Singh, “A high-IIP3 third-order ellipticfilter with current-efficient feedforward-compensated opamps,” IEEETrans. Circuits Syst. II, Exp. Briefs, vol. 58, no. 4, pp. 205–209, Apr. 2011.

[15]. M. Ahmadi, “A new modeling and optimization of gain-boosted cascodeamplifier for high-speed and low-voltage applications,” IEEE Trans.Circuits Syst. II, Exp. Briefs, vol. 53, no. 3, pp. 169–173, Mar. 2006.

[16]. Phuoc T. Tran, Herbert L. Hess, Kenneth V. Noren Operational Amplifier Design with Gain-Enhancement Differential Amplifier 978-1-4673-2421-2/12/$31.00 ©2012 IEEE

**Author's**

**Raghavendra Gupta** has received his Bachelor of Engineering degree in Electronics & communication engineering from Oriental College of Technology (formerly known as Thakral College of Technology), Bhopal in the year 2010. At present he is pursuing M.Tech with the specialization of VLSI Design in, Lakshmi Narain College of Technology, Bhopal. His area of interest Amplifier design, VLSI designing field & Programming Languages.

**Prof. Sunny Jain** has received his Bachelor of Engineering in Electronics & Instrumentation Engineering from JNCT, Bhopal in the year 2009 & has received his M.Tech from OIST, Bhopal with the specialization of Digital Communication. At present he is working as an Assistant Professor In dept. of ECE at , Lakshmi Narain College of Technology, Bhopal. His areas of interests are Power electronics, Digital Communication Field.