Low Power Sram Design Using Multi-Bit Flip-Flop (MBFF)

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ABSTRACT: The increasing demand for battery-powered and green-compliant applications has made power management a dominant factor in SoC design. Clock power contributes 40% of total chip power.To get maximum reduction in power an algorithm has been proposed in which single-bit flip-flops are replaced with maximum possible Multi-Bit Flip-Flop (MBFF) without affecting the performance of the original circuit. Firstly mergable flip-flops are identified based on synchronous clocking and replaced without affecting the performance however replacement will change the location of flip-flops leading to timing and capacity constraint. Tanner EDA V13.0 has been used which reduces the power by 15%.

Keywords: low power, clock power, merging, multi-bit flip-flop, time violation.

1 INTRODUCTION

Power has become one of the main implementation bottlenecks for modern integrated circuit design. In particular, high power consumption may prevent a high-speed design from running at its full speed, while low power dissipation is a must for consumer and portable electronic products[3],[4]. Moreover, the clock signal toggles in each cycle, the total power dissipation in the clock network could be significant.

$$P_{clk} = C_{clk} V_{dd}^2 f_{clk} \quad (1)$$

Where Pclk is clock power

Fclk is the clock frequency

Vdd is the supply voltage

Cclk is the switching capacitance including the gate capacitance. Power consumed by clock plays a dominant role, the clock system consumes 20–45% of the total chip power [7]. Moreover, systems are operating at very high frequencies due to technology advances, which leads to shorter signal transition time. The transition time has effects on power consumption. Therefore the clock distribution needs more careful design planning methodology in low power for modern VLSI. Clock distribution networks, in particular, are an essential element of a synchronous digital circuit and a significant power consumer. Depending on application the clock power varies and in shown in Fig.1.

2 MULTI-BIT FLIP-FLOP

A single-bit flip-flop has two latches (Master latch and slave latch). The latches need Clk and Clk' signal to perform operations. In order to have better delay from Clk-> Q, Clk is regenerated from Clk'. Hence there will be two inverters in the clock path which acts as buffer.Fig.2 shows an example of merging two 1-bit flip-flops into one 2-bit flip-flop. Each 1-bit flip-flop contains two inverters, master-latch and slave-latch. Due to the manufacturing rules, inverters in flip-flops tend to be oversized [8]. As the process technology advances into smaller geometry nodes, the minimum size of clock drivers can drive more than one flip-flop. Merging single-bit flip-flops into one multi-bit flip-flop can avoid duplicate inverters, and lower the total clock dynamic power consumption. The total area contributing to flip-flops can be reduced as well. After the two 1-bit flip-flops are replaced by the 2-bit flip-flop, the wire-lengths of nets are changed. To avoid the timing violation caused by the replacement, the Manhattan distance of new net's cannot be longer than the specified values [5],[6]. A positive edge, master-slave type D flip-flop is composed of two level triggered latches, called master and slave. Basic principle is that second latch (slave) is driven by the clock signal, while the first one (master) is driven by the inverted version of the clock signal. While master latch is transparent and when clock is low, slave latch holds its value and while master latch holds its value, which occurs when clock is high, slave latch becomes transparent, thus making the flip-flop sensitive to low-to-high transition of the clock. There are various ways to implement D latches [4].

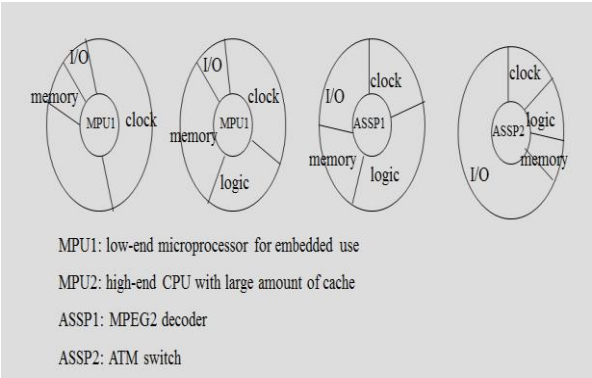

Fig.1. Power distribution in various applications

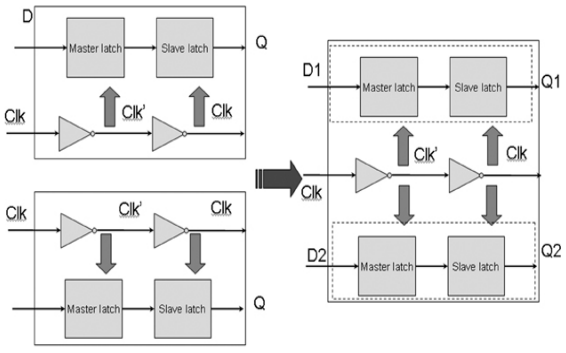

Fig.2 Example of MBFF.

3 Related Work

In Shyu et al. [3] they proposed an algorithm to reduce power consumption of clock by replacing some flip-flops with fewer multi-bit flip-flops. First, the feasible placement regions of a flip-flop associated with different pins are found based on the timing constraints defined on the pins. Then, the legal placement region of the flip-flop fi can be obtained by the overlapped area of these regions. However, because these regions are in the diamond shape, it is not easy to identify the overlapped area. To find the overlapped area they used coordinate transformation technique and got rectangular region. In the second stage, they build a combination table**,** which defines all possible combinations of flip-flops in order to get a new multi-bit flip- flop provided by the library. The flip-flops can be merged with the help of the table. After the legal placement regions of flip-flops are found and the combination table is built, flip-flops can be merged. To speed up the program, they divided a chip into several bins and merged flip-flops in a local bin. They repeated this process by combining bins until no flip-flop can be merged anymore. The limitations of this are they implemented it in C++ which includes complex instruction set, complicated memory management, large execution time and requires additional module for hardware integration.

3 Our Algorithm

The algorithm is roughly divided into two steps. Firstly, mergable flip-flops are identified based on synchronous clocking. Secondly, flip-flops are merged in such a way that the performance of the design is not affected. Single-bit flip-flops can be replaced with multi-bit flip-flops if and only if the library supports it. The library supports only 1-bit, 2-bit and 4-bit flip-flops. However replacement of MBFF induces longer wirelength between flip-flop and its connection pins which introduces larger delay leading to timing constraints as shown in Fig.3. Hence wirelength should be small to get minimum power dissipation. The capacity constraint is also taken in account.

4.1 Timing Constaint Violation

The timing constraint violation can be satisfied by Elmore delay model. The delay of a wire is quadratic function of its length. The network can be either lumped or distributed RC.The delay of distributed RC-line is one-half of the delay predicted in lumped model. The latter combines the total resistance and capacitance into single elements, and has a time-constant equal. For a 10cm long wire of width 1µm the value of R=0.075Ω/µm and C=110aF/µm which produces a delay of 41.3ns for a distributed RC model. However Elmore delay is not equal to delay time [1].

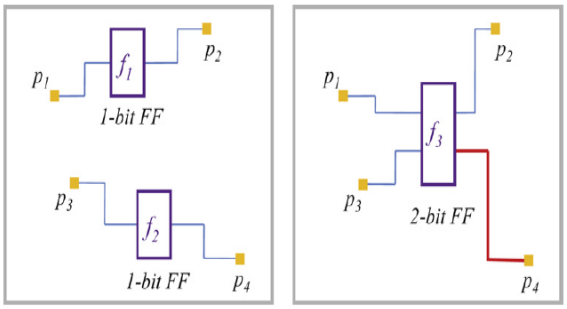

Fig3. Timing Constraint Violation

4.1 SRAM Design

A 4x4 SRAM has been designed which consist of 16 flip-flops in 2D array, it uses 2-to-4 decoder to select a row [2], a single w/R option is used as both write and read signal, when it is ‘0’ write operation will be performed and when it is ‘1’ read operation is been performed, address line is used to select one of the four words and is shown in Fig.4 (a). According to the algorithm flip-flops whose input does not depend on previous output are the flip-flops that can be merged, without affecting the performance of the design and is shown in Fig.4(b) which uses four 4-Bit flip-flops. The output obtained in both the methods is shown in Fig.4(c) which does not affect the performance of the original circuit satisfying the proposed algorithm and capacity constraint

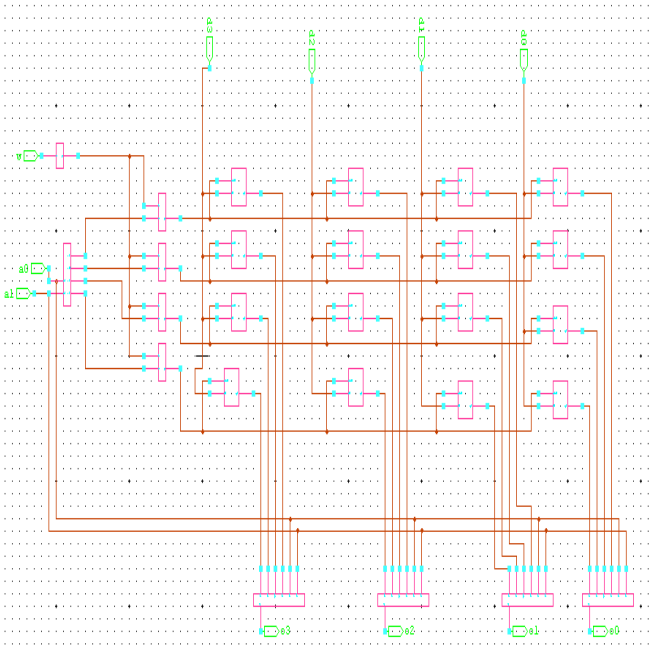

Fig.4 (a) 4x4 SRAM design using Single-Bit FF.

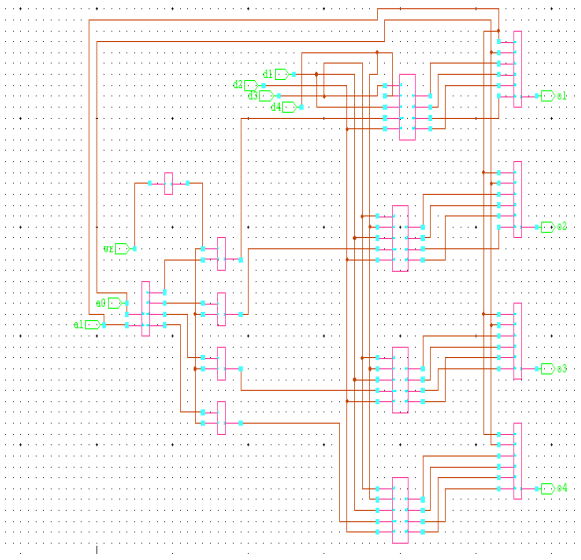

Fig.4 (b) 4x4 SRAM design using MBFF

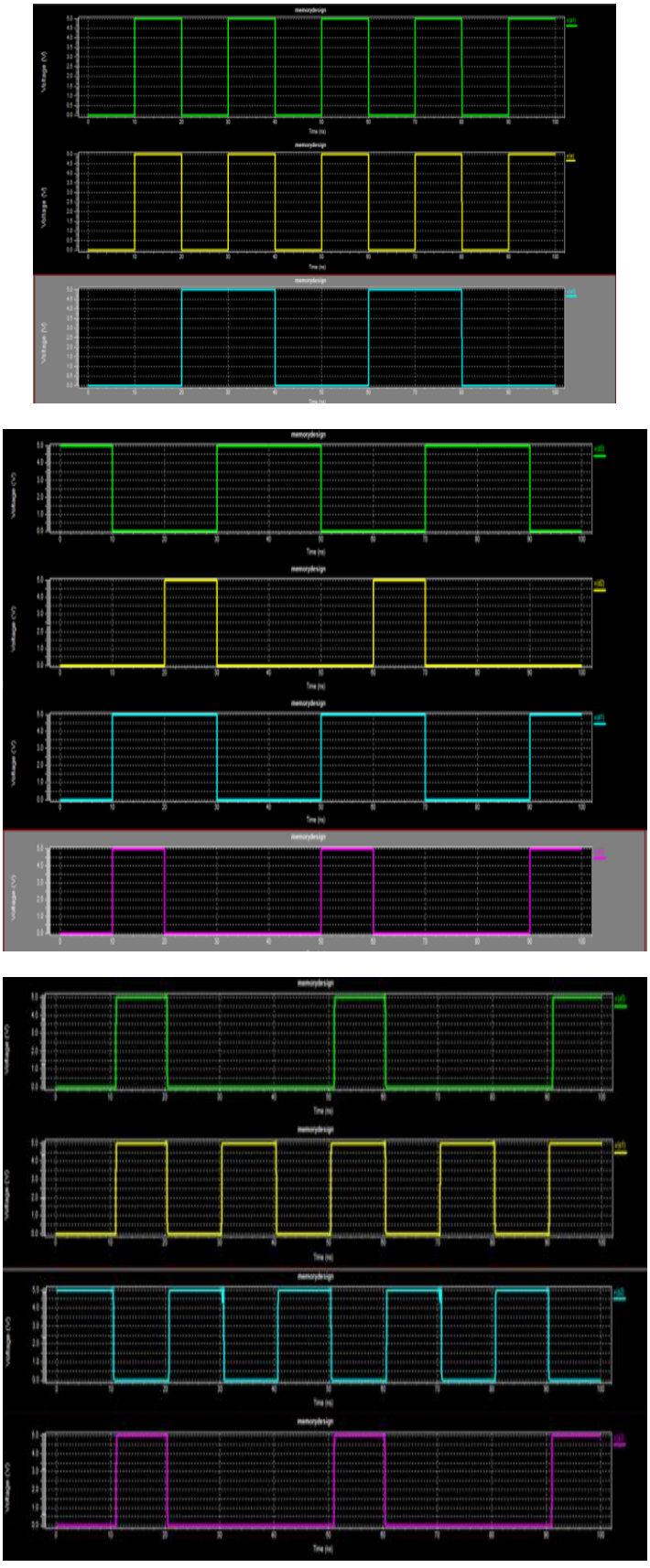

Fig 4(c) Output of 4X4 SRAM

5 Results And Discussion

Power results for multi-bit flip-flop are determined using Tanner Tool v13.0 under 25µm technology at 5V. The power results for 1-bit, 2-bit and 4-bit flip-flops are obtained and the power consumed by single-bit flip-flop is more than that of MBFF.The power result for 4X4 SRAM is shown in TABLE I.

TABLE I
POWER RESULTS OF SRAM

FREQUENCY in GHz	POWER in mW	
50	Single-Bit Flip-Flop	Multi-Bit (4-Bit) Flip-Flop
	30.8	4.8

The power consumed by single-Bit flip-flop is 6times that of Multi-Bit Flip-Flop (MBFF) which gives power reduction ratio[3] of 85% .

6 Conclusion

This paper has proposed an algorithm flip-flop replacement for power reduction in memories. The direct way is to repeatedly search a set of flip-flops that can be replaced by a new multi-bit flip-flop until none can be done. However, as the number of flip-flops in a chip increases the complexity also increase, which makes the method impractical. By the guidelines of replacement from the library, the impossible combination of flip-flops will not be considered since it reduces the execution time. The experimental result shows that our algorithm reduces power by 6 times. Future work involves constructing layout for 4X4 SRAM in Tanner v13.0 and finding wirelength for the Aluminium wire and employing the proposed algorithm for S1423 sequential benchmark circuits which consist of 74 D-flip-flops taken from International Symposium on Circuits and Systems 89 (ISCAS 89) and checking their behavior.

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