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Digital Implementation Of Sinusoidal Pulse Width Modulation Generator

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ABSTRACT: This is the digital implementations of Sinusoidal Pulse Width Modulation (SPWM) generators based on analog circuits. The FPGA based SPWM generator is capable to operate at switching frequencies up to 3 MHz, thus it is capable to support the high switching frequency requirements of modern single-phase dc/ac power converters. The Existing design the switching operation is in 1 MHz. Additionally, in this proposed project it is modified to increase the switching frequency upto 3 MHz and flexible architecture that can be tuned to a variety of single-phase dc/ac inverter applications which exhibits much faster switching frequency, lower power consumption, and higher accuracy of generating the desired SPWM waveform.

Keywords: Sinusoidal Pulse Width Modulation (SPWM), Field Programmable Gate Array (FPGA), Direct Digital Synthesis (DDS), Digital Clock Manager (DCM)

1 INTRODUCTION

THE dc/ac converters (inverters) are the major power electronic conversion units in renewable energy production, motor drive, and uninterruptible power supply applications. A simplified block diagram of a single-phase, full bridge dc/ac power converter (inverter) is depicted. The Sinusoidal Pulse Width Modulation (SPWM) technique is widely employed in order to adjust the dc/ac inverter output voltage amplitude and frequency to the desired value. In this case, the power converter switches are set to the ON or OFF state according to the result of the comparison between a high-frequency, constant-amplitude triangular wave (carrier) with two low-frequencies (e.g., 50 Hz) reference sine waves of adjustable amplitude and/or frequency.

2 EXISTING SYSTEM

The unipolar SPWM technique generate pulses are either positive or negative during each half period of the SPWM wave. Increasing the switching frequency of the triangular wave f_c results in a reduction of the dc/ac inverter output filter size and cost. Depending on their nominal power rating, the dc/ac inverters typically operate at switching frequencies in the range of 1–100 kHz. This trend of increasing the operating switching frequency is expected to continue in the near future due to the recent development of Silicon Carbide power semiconductors, such as JFETs, MOSFETs and Schottky diodes which are capable to operate at switching frequencies up to 3 MHz with low-power losses .The digital SPWM generator implementations have dominated over their counterparts based on analog circuits, since they offer higher noise immunity and less susceptibility to voltage and temperature variations.

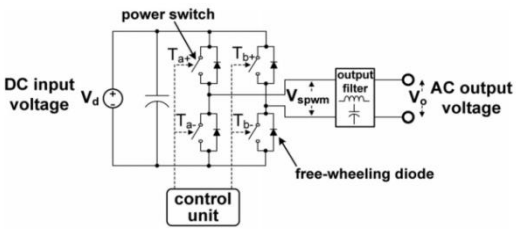

Fig 1: Single-phase DC/AC power converter

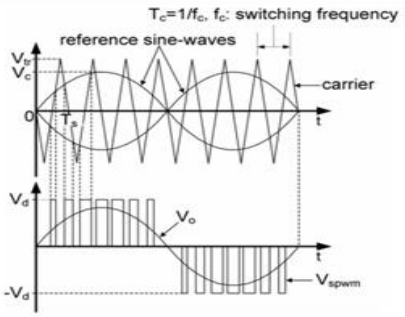

Fig 2: Unipolar SPWM Techniques

2.1 ALGORITHM TECHNIQUE

Targeting at the reduction of the SPWM generator memory requirements, the sinusoidal wave is produced in using an FPGA-based implementation of the Coordinate Rotation Digital Computer (CORDIC) algorithm. A 5-kHz switching frequency has been achieved in this case. Although this implementation does not require the use of a hardware multiplier, it is characterized by a slower speed compared to the LUT-based SPWM units. The CORDIC algorithm has also been applied for the development of an integrated circuit performing the generation of a 5-kHz SPWM wave using 0.18-μm CMOS technology. An LUT is used to store the reference sine-wave digital values corresponding to the time instants of the peaks and nadirs of the triangular wave. The width of each pulse is calculated using an equation based on the similarity of the triangles ABC and ADF depicted in Fig. 3.1. (b). This design method has been validated in case of a 1-kHz switching frequency.

2.2 Direct Digital Synthesis (DDS)

The SPWM pulse train is produced by comparing the sinusoidal and triangular signals generated according to the direct digital synthesis (DDS) technique. The comparison is performed using a high-speed analog comparator. The DDS approach is also used for the development of a digital SPWM generator chip using 0.35-μm CMOS technology. The maximum clock frequency of this chip is 50 MHz. The SPWM unit is composed of a DSP chip accomplishing the calculation of the widths of the individual pulses comprising the SPWM wave,

which communicates through a parallel port with an FPGA-based unit producing the SPWM control signals. The regular-sampled PWM technique presented targets to reduce the amount of computation time required in order to facilitate the generation of higher switching frequencies online and in real time. In this technique, the pulse width is calculated once and used over N consecutive switching edges of the SPWM wave pulses. Then, a new sample of the reference sine wave is acquired. Thus, the sampling frequency f_s is reduced by an integer factor of N, resulting in the following relationship with the corresponding carrier frequency f_c

$$f_s = f_c/N$$

Consequently, the number of calculations required to produce the complete SPWM waveform is N times less than in the conventional SPWM generation methods. A common disadvantage of the previously proposed SPWM generators described previously is that they have been designed to operate at low-switching frequencies, f_c (i.e., 1–20 kHz), while their operation at higher switching frequencies has not been explored yet. In this paper, an FPGA-based SPWM generator is presented, which is capable to operate at switching frequencies up to 1 MHz; thus, it is capable to support the high switching frequency requirements of modern single-phase dc/ac power converters. Compared to the past-proposed SPWM generators, in the proposed architecture the values of both the reference sine and triangular waves are stored in the FPGA device Block RAMs (BRAMs) in order to exploit their one-clock cycle access time, thus providing a much higher switching frequency capability. The proposed design exhibits architectural flexibility features, enabling the change of the SPWM switching frequency and modulation index either internally, or externally. The proposed SPWM unit has been implemented in a single chip in order to enable the reduction of the complexity, cost, and development time of the dc/ac inverter control unit.

2.3 SPWM Generator

The architecture of the proposed SPWM generation unit is presented. The system inputs are the modulation index of the output SPWM wave M in single precision floating point arithmetic ranging from 0 to 1, as well as the “clock” and “reset” signals. The architecture of the proposed system has been built using 8-bit fixed-point arithmetic and it consists of five subsystems, which implement the SPWM generation algorithm.

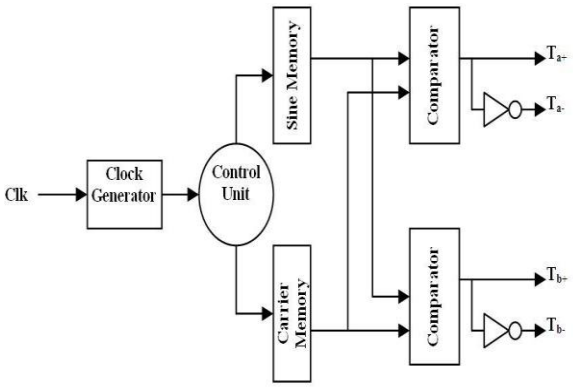

Fig 3: Architecture of the proposed SPWM generation unit.

3 SPWM GENERATOR SUBSYTEM

3.1 Clock Generator Subsystem

The “Clock generator” subsystem takes as input the FPGA input clock and produces a new clock signal used by the digital circuits of the proposed SPWM generator, such that the desired SPWM switching frequency fc specified by the designer/user is generated. A two-state finite state machine (FSM) is initially used to set the input clock frequency f clk to f clk/2 and then a Digital Clock Manager module adapts this frequency to the desired value. The Very high speed integrated circuit Hardware Description Language (VHDL) code of the DCM module. The FSM is kept constant for every different switching frequency, while only the operational parameters “CLKFX_MULTIPLY” and “CLKFX_DIVIDE” of the DCM module are changed according to the switching frequency requirements of the SPWM output waveform. Thus, the proposed SPWM generator is flexible to be adapted to the generation of any operating switching frequency specified by the system designer/user.

3.2 Sine-Carrier Subsystem

The “Sine-Carrier” subsystem consists of the control unit, two BRAMs, which contain samples of the sinusoidal and triangular (i.e., carrier) waves and two multiplexers that produce the two constant-amplitude reference sine waves used for the production of the SPWM output signals. The BRAMs of the sine wave and carrier operate as LUTs. Both the sinusoidal and triangular waves are sampled and quantized with the same sampling frequency fs using MATLAB (e.g., fs = 4, 8 MHz, etc.). In order to minimize the utilization of the FPGA resources, only the values of the first quarter of the constant-amplitude sine-wave period (i.e., during the time interval 0 − π/2) are stored in the corresponding BRAM, while the values of the sine wave during the time interval π/2 − 2π are calculated by mirroring and inverting the values of the first quarter. The BRAM of the carrier contains the values of a complete period of the reference triangular wave. Consecutive addresses of both memories (“Sine address” and “Carrier address,” respectively) are generated in every clock cycle by the control unit. The control unit also produces a “flag” signal, which is responsible.

3.3 Adjustable Amplitude Sine Subsystem

The “Adjustable amplitude sine” subsystem takes as input the constant-amplitude reference sinusoidal values produced by the “Sine-Carrier” subsystem and generates a sinusoidal digital signal ya with amplitude adjustable according to the value of the modulation index M which is an input in the proposed SPWM generation system. The value of ya is in the range 0–255 and it is calculated and the value of the constant-amplitude reference sine wave and Index is the output of the “Modulation Index” subsystem.

3.4 Comparison Subsytem

The “Comparison” subsystem implements the comparison between the high-frequency constant-amplitude triangular waves (carrier) with the two low-frequency reference sine waves, using two comparators (“COMP”). The control signals Ta+, Ta−, Tb+, and Tb− of the single-phase dc/ac inverter power switches depicted are generated from the outputs of the corresponding comparators of this subsystem, thus forming the SPWM wave (Vspwm) at the dc/ac inverter output

terminals. The outputs of the comparators in the Comparison" subsystem (i.e., control signals Ta+ and Tb+) are equal to one when the corresponding output of the "Adjustable amplitude sine" subsystem described in Section II- by inverting Ta+ and Tb+, respectively. C is equal to or greater than the current digital value of the carrier signal. The DC/AC inverter control signals Ta− and Tb− are produced

4 Proposed System

An FPGA-based SPWM generator has been presented, which is capable to operate at switching frequencies up to 1 MHz, thus it is able to support the high switching frequency requirements of modern single-phase dc/ac inverters. The proposed design occupies a small fraction of a medium sized FPGA and, thus, can be incorporated in larger design, while it has a flexible architecture can be adapted to a variety of single-phase dc/ac inverter applications. Both post place and route simulation results and experimental verification results on actual hardware were presented, demonstrating the successful operation of the proposed SPWM generator at high switching frequencies. The proposed SPWM generation techniques were also implemented and their performance was compared. The post layout simulation and experimental results confirm that the proposed SPWM generator exhibits much faster switching frequency, lower power consumption, and higher accuracy of generating the desired SPWM waveform.

5 Simulation Results

The proposed network design configured with a 4-bit data width is simulated by using ModelSim SE 6.3 tool. The 4-bit data width is chosen mainly for testing purpose, data width can be easily sized according to the requirements of real applications. Three kinds of switches are designed for the proposed on-chip network. These switches are all based on common switch architecture and the single switch simulation result is shown.

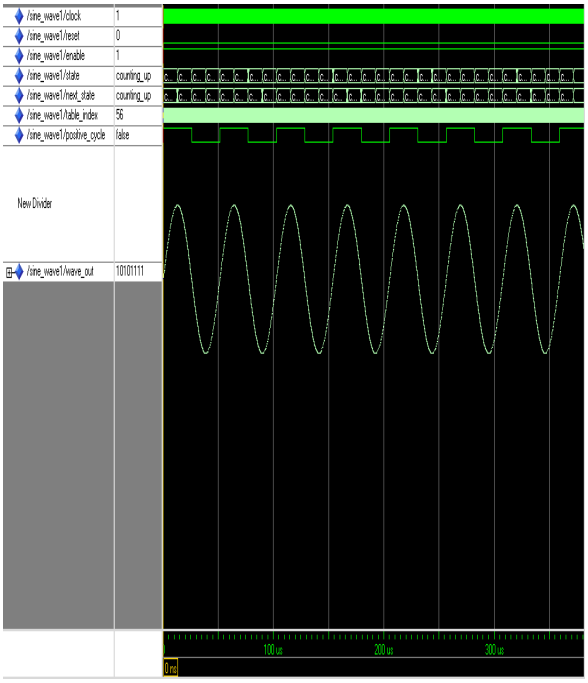

Fig 4: sine wave generation

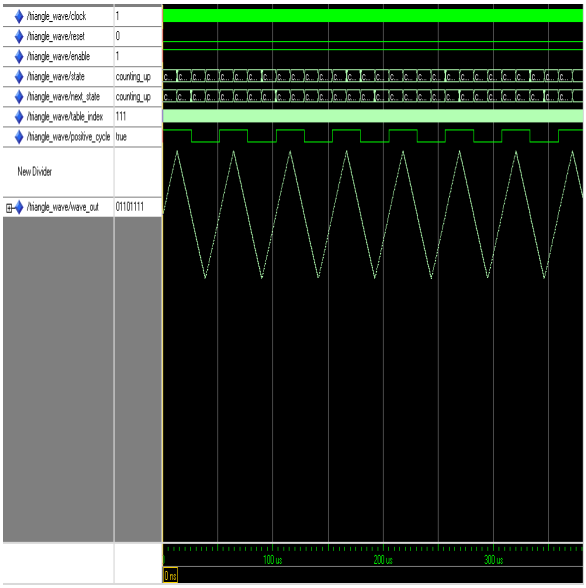

Fig 5: Triangular (Carrier) wave generation

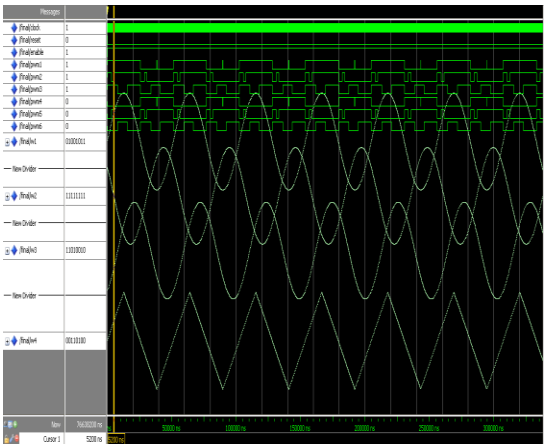

Fig6: Output waveform of Comparison of Sine wave with reference carrier waveform

6 Future Work

In the existing work by Improvement in Design of Control Circuit to increase the frequency up to 3Mhz and reduce power consumption of Sinusoidal Pulse Width Modulation (SPWM) Generator.

7 Conclusion

The SPWM principle is widely used in dc/ac inverters in energy conversion and motor drive applications. The past proposed SPWM generators have been designed to operate at low switching frequencies (i.e., 1–20 kHz), while their operation at higher switching frequencies had not been explored so far.

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